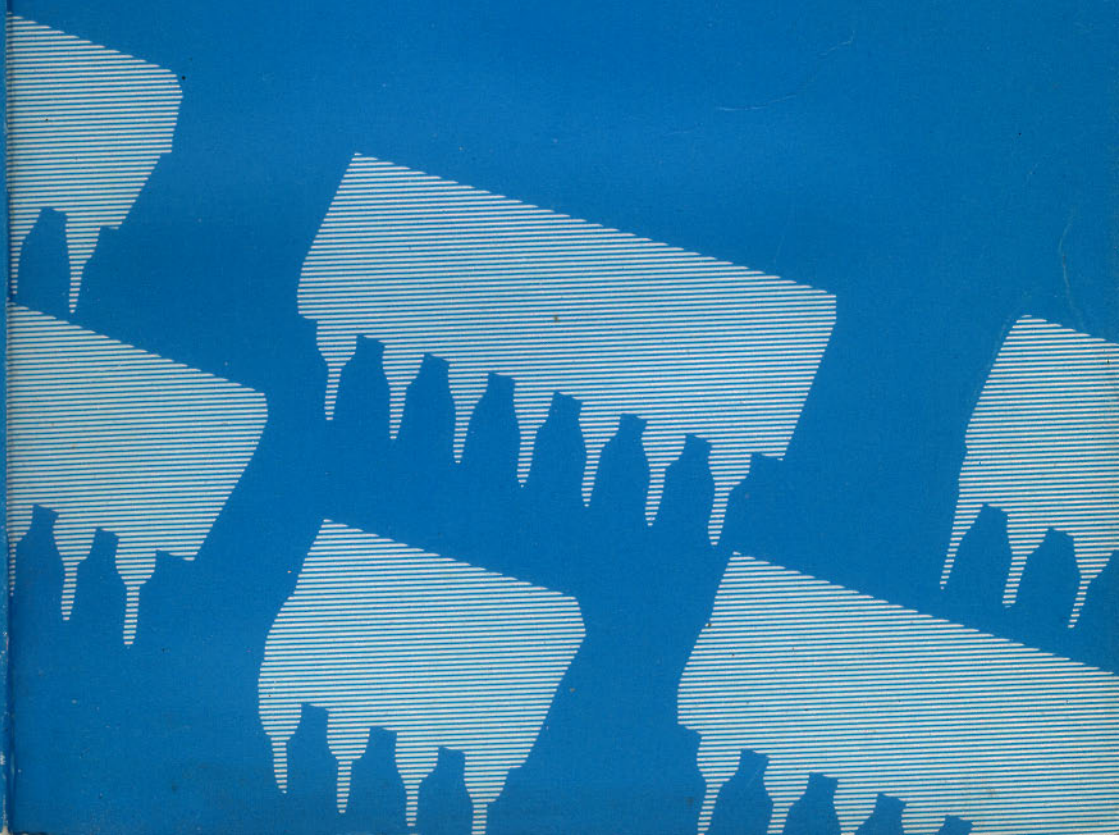
LINEAR INTEGRATED CIRCUIT HANDBOOK

PLESSEY
Semiconductors



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Designed and produced by Peter Wigens Consultants

March 1983
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Contents

Product index

POWER CONTROL CIRCUITS

Product list

Quality data

Plessey Semiconductors has Factory Approval to:-

BS9300 for semiconductor devices of Assessed Quality (BSI Certificate 1053/M)

BS9400 for integrated circuits of Assessed Quality (BSI Certificate 1053/M)

CECC 50000 Inspection Organisation to document level 1 (BS9300) M0020/CECC refers

DEF STAN 05 — 21 QC System requirements for Industry (Equivalent to AQAP — 1) Certificate 65752/1/01 refers

Devices are also manufactured and tested in accordance with the methods of **MIL-STD-833**, the US Military Standard; Test Methods and Procedures for Microcircuits, and **MIL-M-38510**, US Military Specification, Micro-electronics; General Specifications for.

Ordering information

All Plessey Semiconductors integrated circuits are allocated type numbers which must be quoted when ordering. This number may or may not have a suffix (A, B, C, etc.) which denotes the precise electrical specification or temperature grade. When there is a choice of packages the two-digit Pro-Electron code is used to identify the style required, according to the following table:

CM - Multilead TO-5
DC - Ceramic Dual-in-Line (metal lid)
DG - Ceramic Dual-in-Line
GC - Ceramic Chip Cover

Within the UK, orders for quantities up to 99 will be referred to your local Distributor. Quantities of 1000 and over must be ordered from:

Plessey Semiconductors Limited
Cheney Manor
Swindon, Wiltshire SN2 2QW
United Kingdom
Telephone: Swindon (0793) 36251
Telex: 449637

A reciprocal arrangement exists with all Distributors, but it will expedite delivery of order if buyers can direct orders as indicated above. Outside the UK, irrespective of quantity, you are invited to contact your nearest Plessey Semiconductors Sales Outlet (see pages 203-207).

DELIVERED PRODUCT QUALITY

It is our policy to deliver a reliable quality product and to achieve this end all devices undergo 100% electrical testing of every relevant AC and DC parameter prior to shipment. The devices are tested under conditions of level and frequency closely simulating those of the typical application. Fully automatic Teradyne integrated circuit test machines, acknowledged to be among the best computer controlled test machines available, are employed.

Each and every stage of processing, assembly and testing is carefully audited by Plessey Semiconductors' independent Quality Assurance department.

Therefore we are able to guarantee the following Acceptable Quality Level (A.Q.L.) on all deliveries.

MECHANICAL

Defects of a mechanical nature including coding not being legible, deformed leads, dimensional tolerances being exceeded, wrong identification of pin 1 and pins not being solderable.

0.65% AQL,I.L.II

ELECTRICAL

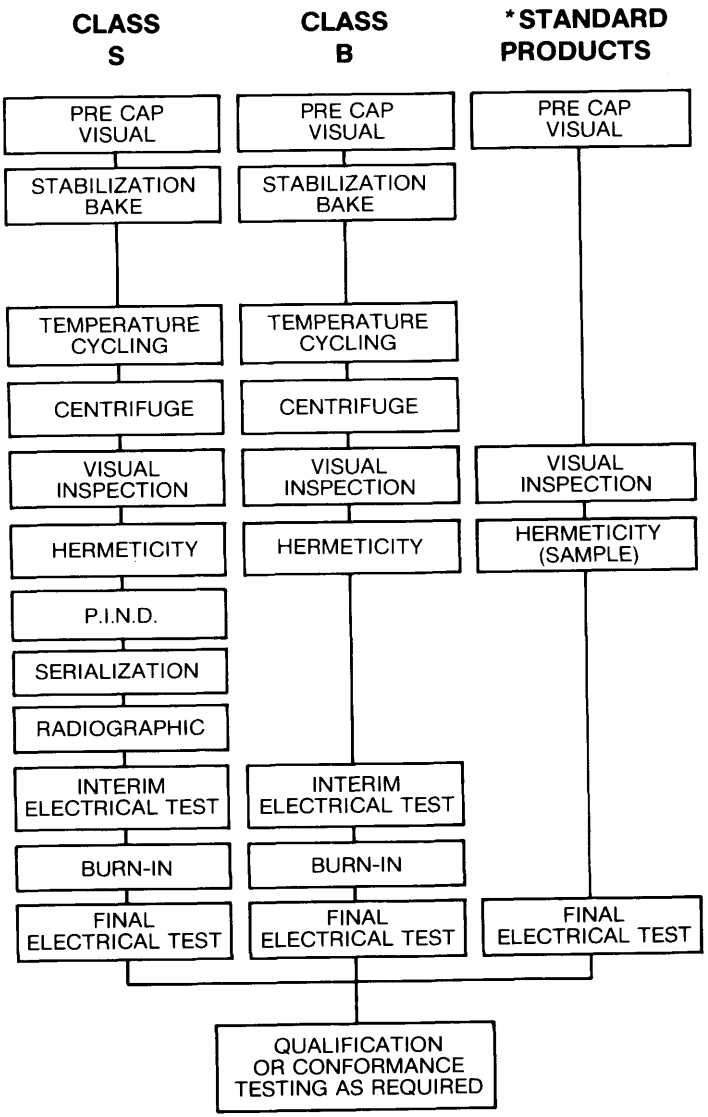
Defects of an electrical nature including device parameters being outside the acceptance specification limits, or those only stated as typical being grossly in error.

0.4% AQL,I.L.II

The average delivered product quality is considerably better than this, the population of imperfect devices being much smaller than that indicated by the AQL values.

Screening to MIL-STD-883

The following Screening Procedures are available from Plessey Semiconductors



*Plessey Semiconductors reserve the right to change the Screening Procedure for Standard Products.

Semi-custom design

The table outlines the essential parameters of our Semi-custom design techniques, including typical timescales for the design and production of a Semi-custom IC.

NAME	PART NUMBER	TECHNOLOGY	LOGIC ELEMENTS	TYP.GATE DELAY/POWER	SYSTEM CLOCK SPEED
Microcell	MJ 1XXX	NMOS (Std)	Up to 3000 equiv.gates	50ns at 250μW	2MHz
	MJ 1XXX	NMOS (low power)	Up to 3000 equiv.gates	200ns at 40μW	2MHz
	MV 1XXX	CMOS	Up to 2000 equiv.gates	20ns at 12μW/MHz	8MHz
Microgate-C 1000 Series (CMOS Gate Array)	CLA 10XX	CMOS	560	6ns at 6μW/MHz	8MHz
	CLA 12XX	CMOS	960	6ns at 6μW/MHz	8MHz
	CLA 15XX	CMOS	1440	6ns at 6μW/MHz	8MHz
Microgate-C 2000 Series (CMOS Gate Array)	CLA 21XX	CMOS	840	4ns at 3μW/MHz	14MHz
	CLA 23XX	CMOS	1440	4ns at 3μW/MHz	14MHz
	CLA 25XX	CMOS	2400	4ns at 3μW/MHz	14MHz
Microgate-E (ECL Gate Array)	SCD 1XXX	ECL	75	550ps/900mW	300MHz
	SCD 2XXXH	ECL	300	550ps/3.5W	300MHz
	SCD 2XXXM	ECL	300	1.5ns/1W	250MHz
	SCD 2XXXL	ECL	300	2ns/750mW	100MHz

NAME	PART NUMBER	TECHNOLOGY	COMPONENT COUNT		
			RESISTANCE	TRANSISTORS	
				NPN	PNP
Microlin (Analogue Array)	BAA 1XXX	Bipolar	1219kΩ	81	28
	BAA 2XXX	Bipolar	2757kΩ	163	58

*Design and test times given are typical. Actual times will depend on the complexity of the particular circuit.

INPUT/ OUTPUT ELEMENTS	COMPATI-BILITY	MAX. PIN COUNT	No. OF CUSTOM MASKS	TYPICAL TIME FOR 1st SAMPLES
As required	TTL/CMOS	64	6	19 weeks *
As required	TTL/CMOS	64	6	
As required	TTL/CMOS	64	9	
38 I or O	TTL/CMOS	40	1	16 weeks *
50 I or O	TTL/CMOS	64	1	
60 I or O	TTL/CMOS	64	1	
40 I or O	TTL/CMOS	44	3	13 weeks *
52 I or O	TTL/CMOS	56	3	
60 I or O	TTL/CMOS	64	3	
25 I or O	ECL 10K	28	3	16 weeks *
36 I 20 I or O	ECL 10K	64	3	
36 I 20 I or O	ECL 10K	64	3	
36 I 20 I or O	ECL 10K	64	3	

f_T (1mA 5V Vcc) STANDARD NPN	LV_{CEO}/ BV_{CEO}	MAX. PIN COUNT	No. OF CUSTOM MASKS	TYPICAL TIME FOR 1st SAMPLES
470MHz	20V/30V	24	1	15 weeks *
470MHz	20V/30V	24	1	

Technical Data

PLESSEY
Semiconductors

SL301K, SL301L

400MHz DUAL NPN TRANSISTOR

The SL301K and SL301L are dual monolithic NPN transistors with close parameter matching and high f_T. The SL301K and SL301L have identical electrical specification.

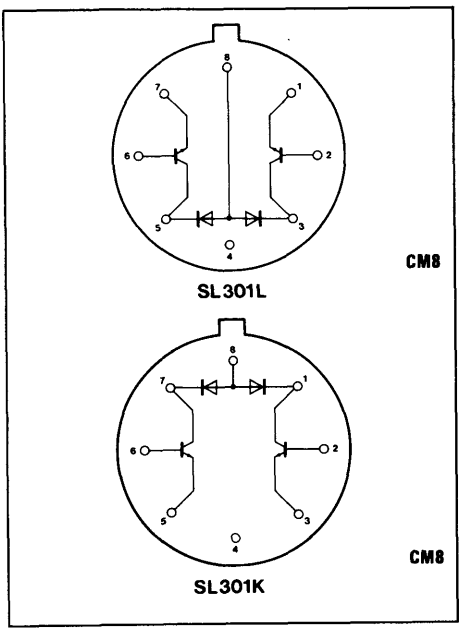


Fig.1 Pin connections

FEATURES

- Close V_{BE} Matching<3mV
- Close h_{fe} Matching>0.9
- Good Frequency Response>400MHz
- Good Thermal Tracking
- Wide Operating Current Range

APPLICATIONS

- Differential Amplifier to Very High Frequencies
- Comparators
- Current Sources
- Instrumentation

ABSOLUTE MAXIMUM RATINGS

All electrical ratings apply to individual transistors. Thermal ratings apply to the total package.

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

The isolation pin (substrate) must be connected to the most negative point of the circuit to maintain electrical isolation between transistors.

Storage temperature -55°C to +175°C (CM8)
Maximum junction temperature +175°C
Thermal resistance: see Note 1
Chip-to-case 265° C/W (CM8)
Chip-to-ambient 425° C/W (CM8)

V_{CB} = 20V V_{EB} = 4.0V V_{CER} = 20V (see Fig.7)
V_{CE} = 12V V_{CI} = 25V I_C = 20mA

NOTE:
These figures are worst case, assuming all the power is dissipated in one transistor. If the power is equally shared between the two transistors, both thermal resistance figures can be reduced by 50°C/watt.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = 22°C \pm 2°C$

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Collector base breakdown	BV_{CBO}	20			V	$I_C = 10\mu A$
Collector emitter breakdown	BV_{CEO}	12			V	$I_C = 10\mu A$
Collector emitter breakdown	LV_{CEO}	12			V	$I_C = 5mA$
Emitter base leakage current	I_{EBO}			1	μA	$V_{EB} = 4V$
Emitter base leakage current	I_{EBO}			10	nA	$V_{EB} = 2V$
Collector isolation breakdown	BV_{CIO}	25			V	$I_C = 10\mu A$
Forward current transfer ratio	H_{FE}	40	70			$V_{CE} = 5V$, $I_C = 100\mu A$
		60	100			$V_{CE} = 5V$, $I_C = 1mA$
		50	80			$V_{CE} = 5V$, $I_C = 10mA$
Saturation voltage	$V_{CE(SAT)}$		0.36	0.6	V	$I_C = 10mA$, $I_B = 1mA$
	$V_{BE(SAT)}$	0.7	0.8	0.9	V	$I_C = 10mA$, $I_B = 1mA$
Collector base leakage current	I_{CBO}			10	nA	$V_{CB} = 10V$
Collector isolation leakage current	I_{CIO}			10	nA	$V_{CI} = 10V$
Collector capacitance	C_{OB}			2	pF	$V_{CB} = 5V$
Base capacitance	C_{IB}			4	pF	$V_{BE} = 0V$
Collector isolation capacitance	C_{CI}			6	pF	$V_{CI} = +5V$
Transition frequency	f_T	400	680		MHz	$V_{CE} = 5V$, $I_C = 5mA$, Freq = 100MHz
Matching						
H_{FE1}/H_{FE2}		0.9		1.1		$V_{CE} = 5V$, $I_C = 100\mu A$
		0.9		1.1		$V_{CE} = 5V$, $I_C = 1mA$
$\lvert V_{BE1} - V_{BE2} \rvert$	ΔV_{BE}		0.45	3	mV	$V_{CE} = 5V$, $I_C = 100\mu A$
			0.45	3	mV	$V_{CE} = 5V$, $I_C = 1mA$
Temperature coefficient of ΔV_{BE}			2	10	$\mu V/°C$	$V_{CE} = 5V$, $I_C = 100\mu A$

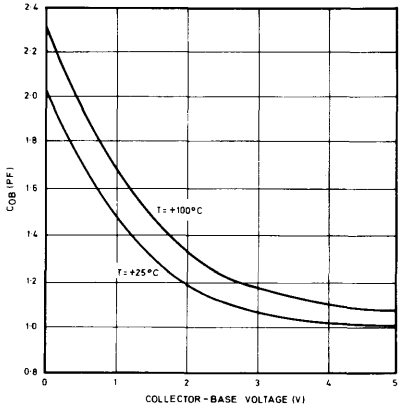


Fig. 2 Output capacitance (C_{ob}) v. voltage

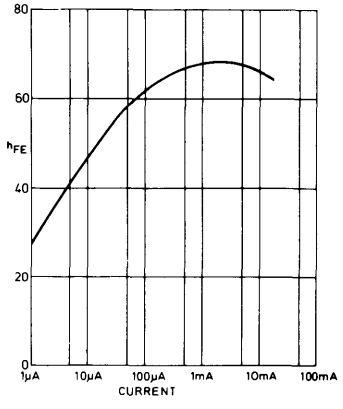


Fig. 3 Typical variation of h_{FE} with collector current

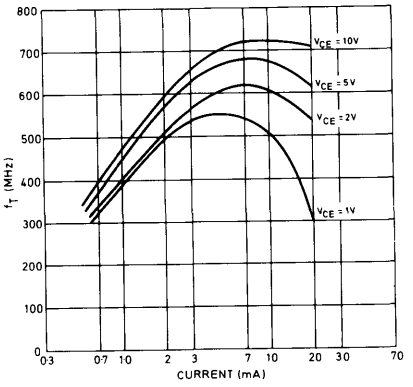


Fig. 4 f_T v. collector curent ($f_T = f\, h_{fe}$. f= 100MHz

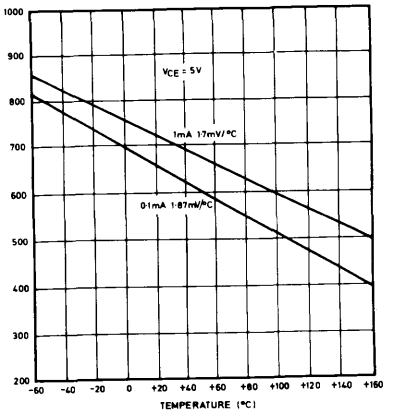


Fig. 5 V_{BE} v. temperature

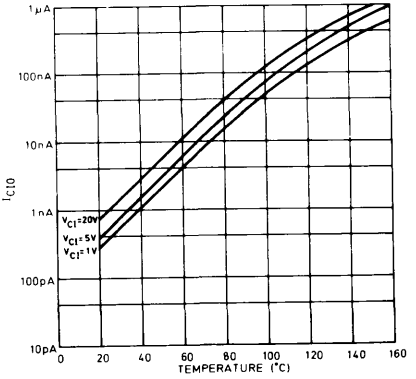


Fig. 6 Typical I_{CIO} v. temperature

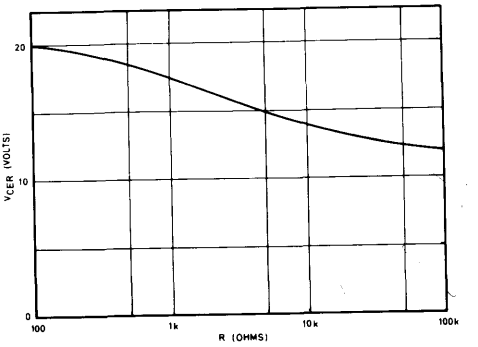


Fig. 7 Relationship between V_{CER} and R_{BE}

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SL303L

400MHz TRIPLE NPN TRANSISTORS

The SL303 is a silicon monolithic integrated circuit comprising three separate transistors, two of which have closely matched parameters; the third transistor may be used as, for example, a tail transistor. The SL303 devices are available in a 10-lead TO—5 (CM) package.

ORDERING CODES: SL303L — CM

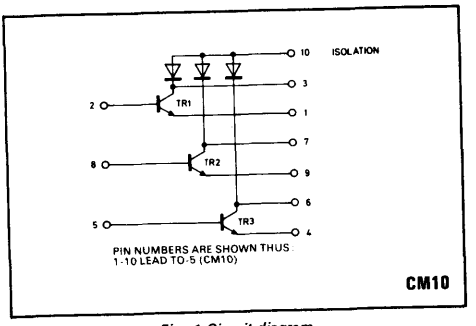

Fig. 1 Circuit diagram

FEATURES

- Close V_{BE} Matching
- High Gain
- Good Frequency Response
- Excellent Thermal Tracking

APPLICATIONS

- Differential Amplifier
- Comparator

QUICK REFERENCE DATA

Max voltage	12V to 20V
Operating temperature range	−55°C to +175°C

ABSOLUTE MAXIMUM RATINGS

All electrical ratings apply to individual transistors: thermal ratings apply to total package dissipation.

The isolation pin must always be negative with respect to the collectors.

No one transistor may dissipate more than 75% of the total power.

Storage temperature	−55°C to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance:	
TO-5 (CM)	425° C/W } see Note 1
Chip-to-case thermal resistance:	}
TO-5 (CM)	265° C/W }
V_{CBO}	20V
V_{CEO}	12V
V_{CER}	12V to 20V (see Figure 8)
V_{EBO}	4V
V_{CIO}	25V
I_{CM}	20mA

NOTE:
These figures are worst case, assuming all the power is dissipated in one transistor. If the power is equally shared between the three transistors, both thermal resistance figures can be reduced by 75° C/watt.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Collector base breakdown	BV_{CBO}	20			V	I_C = 10μA
Collector emitter breakdown	BV_{CEO}	12			V	I_C = 5mA
Emitter base leakage current	I_{EBO}			1	μA	V_{EB} = 4V
Emitter base leakage current	I_{EBO}			10	nA	V_{EB} = 2V
Collector isolation breakdown	BV_{CIO}	25			V	I_C = 10μA
Forward current transfer ratio	H_{FE}	30	50			V_{CE} = 5V, I_C = 10μA
		40	70			V_{CE} = 5V, I_C = 100μA
		60	100			V_{CE} = 5V, I_C = 1mA
		50	80			V_{CE} = 5V, I_C = 10mA
Saturation voltage	$V_{CE(SAT)}$		0.36	0.6	V	I_C = 10mA, I_B = 1mA
	$V_{BE(SAT)}$	0.7	0.8	0.9	V	I_C = 10mA, I_B = 1mA
Base emitter saturation voltage				10	nA	V_{CB} = 10V
Collector base leakage current	I_{CBO}			10	nA	V_{CB} = 10V
Collector isolation leakage current	I_{CIO}			10	nA	V_{CI} = 10V
Collector capacitance	C_{OB}			2	pF	V_{CB} = 5V
Base capacitance	C_{IB}			4	pF	V_{BE} = 0V
Collector isolation capacitance	C_{CIO}			6	pF	V_{CI} = +5V
Transition frequency	f_T	400	680		MHz	V_{CE} = 5V, I_C = 5mA
Matching						
TR1 & TR2 only						
H_{FE1}/H_{FE2}		0.9		1.1		V_{CE} = 5V, I_C = 100μA
		0.9		1.1		V_{CE} = 5V, I_C = 1mA
Input offset voltage	ΔV_{BE}			3	mV	V_{CE} = 5V, I_C = 100μA
				3	mV	V_{CE} = 5V, I_C = 1mA
Temperature coefficient of ΔV_{BE} of input offset voltage	T_{amb}			10	μV/°C	V_{CE} = 5V, I_C = 100μA

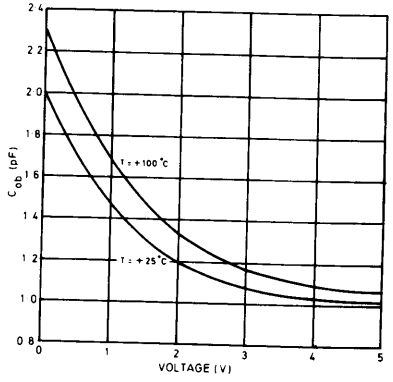

Fig. 2 Output capacitance (C_{ob}) v. voltage

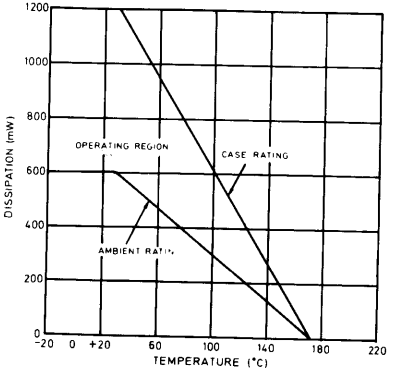

Fig. 3 Power dissipation derating curves (TO-5 package)

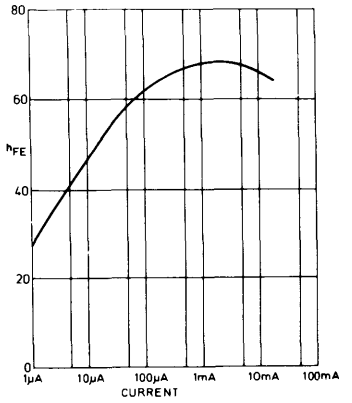

Fig. 4 Typical variation of h_{FE} with collector current

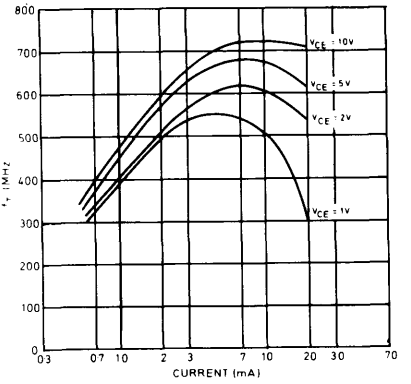

Fig. 5 f_T v. collector current ($f_T = f|h_{fe}|$. f = 100 MHz)

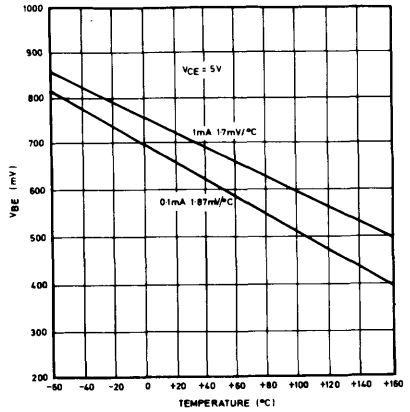

Fig. 6 V_{BE} v. temperature

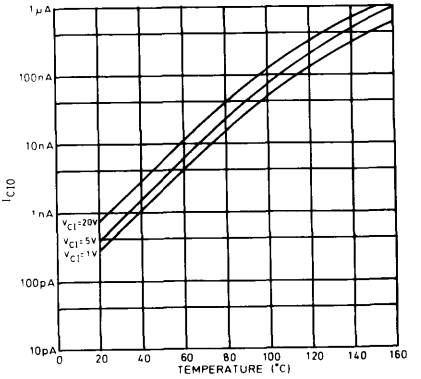

Fig. 7 Typical I_{CIO} v. temperature

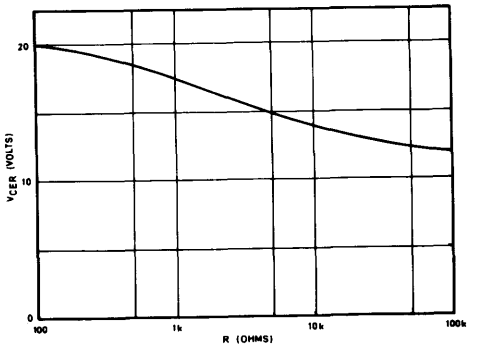

Fig.8 Relationship between V_{CER} and R_{BE}

PLESSEY
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SL360C & SL362C

HIGH PERFORMANCE NPN DUAL TRANSISTOR ARRAYS

The SL360C and SL362C are high performance NPN dual transistor arrays fabricated as monolithic silicon devices. They feature accurate parameter matching and close thermal tracking. They have high transition frequencies (typ. 2.2GHz) and low device capacitance. In addition the SL362C offers good noise performance (1.6dB noise figure at 60MHz).

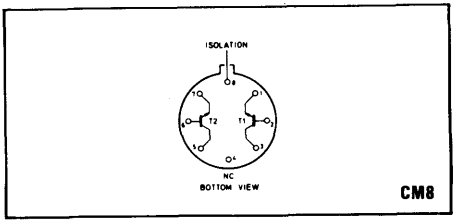


Fig. 1 Pin connections

APPLICATIONS

- Instrumentation
- PCM Repeaters
- Analogue Signal Processing
- High Speed Switches – Digital and Analogue

FEATURES

- Accurate Parameter Matching.
- High f_T (1.5GHz min., SL360)
- Low Noise (1.6dB at 60MHz SL362)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 22°C ± 2°C

Characteristic	Symbol	Type	Value			Units	Conditions
			Min.	Typ.	Max.		
Collector base breakdown	BV_{CBO}	All	10	32		V	I_C = 10μA
Collector isolation breakdown	BV_{CIO}	All	16	60		V	I_C = 10μ
Emitter base leakage	I_{EBO}	SL360/362C			1	μA	V_{EB} = 4V
Emitter base leakage	I_{EBO}	SL360C			1	nA	V_{EB} = 2V
Collector emitter breakdown	LV_{CEO}	All	7	14		V	I_C = 5mA
DC current gain	H_{FE}	SL360C	30	65			V_{CE} = 2V,I_E = 5mA
		SL362C	30	70			V_{CE} = 2V,I_E = 1mA
Transition frequency	f_T	SL360C	1.5	2.2		GHz	V_{CE} = 2.5V,I_E = 5mA,f = 200MHz
		SL360E	1.6	3.2		GHz	V_{CE} = 5V,I_E = 20mA
		SL360G	1.4	2.2		GHz	V_{CE} = 5.0V,I_F = 5mA,f = 200MHz
Input offset voltage	V_{BE1} - V_{BE2}	SL360C		3	10	mV	V_{CE} = 2V,I_F = 1mA
		SL362C		5		mV	V_{CE} = 2V,I_E = 1mA
Input offset current	H_{FE1}/H_{FE2}	All	0.9	1.0	1.1		V_{CE} = 2V,I_E = 5mA
Saturation voltage	$V_{CE}(SAT)$	SL360C		0.25	0.6	V	I_E = 10mA,I_B = 1mA
Noise figure	NF	SL362C		1.6	2.0	dB	I_E = 1mA,R_S = 200Ω,f = 60MHz
Collector base capacitance	C_{OB}	SL360C		0.5		pF	V_{CB} = 0V
		SL362C		1.3		pF	V_{CB} = 0V
Collector isolation capacitance	C_{CI}	SL360C		2.3		pF	V_{CI} = 0V
		SL362C		3.8		pF	V_{CI} = 0V
Emitter base capacitance	C_{TE}	SL360C		0.5		pF	V_{BE} = 0V
		SL362C		2.1		pF	V_{BE} = 0V
Forward base emitter voltage	$V_{BE}(ON)$	SL360C		0.72		V	I_E = 1mA,V_{CE} = 2V
Collector base leakage	I_{CBO}	SL360C			1	nA	V_{CB} = 10V
Collector isolation leakage	I_{CIO}	SL360C			1	nA	V_{CI} = 10V

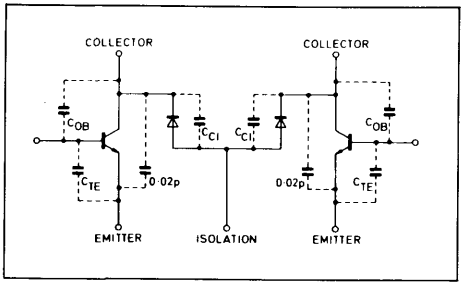


Fig.2 Equivalent circuit for SL360, SL362

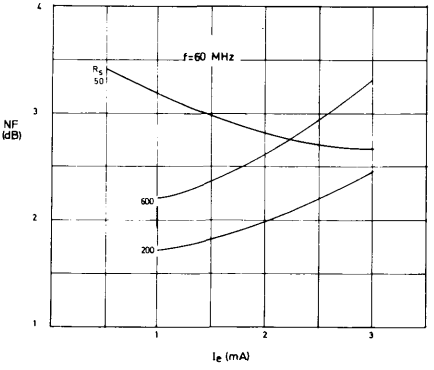


Fig. 3 Typical noise figure emitter current for SL362

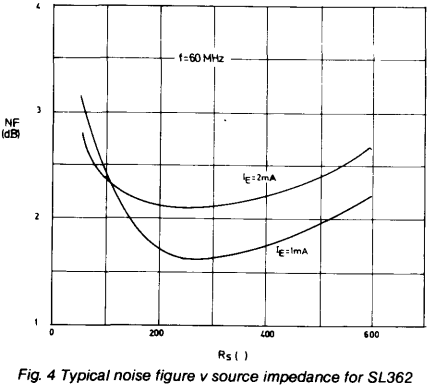


Fig. 4 Typical noise figure v source impedance for SL362

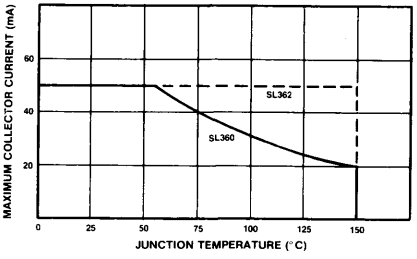


Fig.5 Max. continuous collector current vs junction temperature

ABSOLUTE MAXIMUM RATINGS

All electrical ratings apply to individual transistors. Thermal ratings apply to the total package.

The absolute maximum ratings are limiting values above which life may be shortened or specified parameters may be degraded.

The isolation pin (substrate) must be connected to the most negative point of the circuit to maintain electrical isolation between transistors.

Electrical ratings

V_{CB} = 10V V_{EB} = 4V V_{CE} = 8V
V_{CI} = 16V I_C = 20mA (SL360); 50mA (SL362) (see Figure 5)

Thermal ratings

	CM8
Storage temperature	−55°C to +150°C
Operating junction temperature	150°C
Thermal resistance (see Note 2)	
Chip-to-case	265° C/W
Chip-to-ambient	425° C/W

NOTES
1. The SL360G is also available to order. This meets RC5544 telecommunications requirements. SL360G has the SL360C characteristics with an additional f_T guarantee as shown.
2. These figures are worst case, assuming all power is dissipated in one transistor. If the power is equally shared between the two transistors, both thermal resistance figures can be reduced by 50° C/watt.

PLESSEY
Semiconductors

SL440

POWER CONTROL CIRCUIT

The SL440 is a versatile integrated circuit designed to provide variable-phase control of triacs and other power switching devices in a variety of domestic and industrial applications. The basic elements of the SL440 are shown in Fig.2.

An external timing capacitor, C_T, connected to pin 14 is discharged during positive and negative half cycles of the driving waveform (typically 50 Hz), at a constant rate which is proportional to the output of the servo amplifier (pin 13). When the charge reaches an internally-defined level, the conduction control circuit generates a 50μs (typ.) firing pulse (pin 1) to trigger the triac. The crossover detector resets the timing cycle when the driving waveform passes through zero, at which point C_T is recharged rapidly. The servo amplifier thus controls the conduction time of the triac, and hence the power delivered to the load.

If the Inhibit input (pin 4) is taken below +5V (e.g. to pin 11) the conduction control circuit action is over-ridden and the firing pulses are inhibited. This facility can be used in conjunction with the current limit detector, by driving the AC input terminals (pins 5 and 10) from a current transformer in series with the load. If a load resistor is connected from pin 4 to the stabilised supply (pin 3), a DC voltage, inversely proportional to the AC load current, appears on pin 4. This is applied to the variable delay pulse generator as soon as the internally defined threshold voltage (approximately 5V) exceeds it, and so limits the load current.

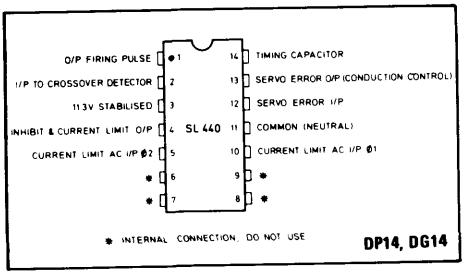


Fig.1 Pin connections (top)

FEATURES

- Conduction Control
- Crossover Detector
- Servo Amplifier
- Internal Stabilised Supply (Available for External Circuitry)
- Total Power Shut-Down Facility
- AC Load Current Limitation

APPLICATIONS

- Lamp Dimmers
- Automatic Lamp Faders
- Motor Speed Control

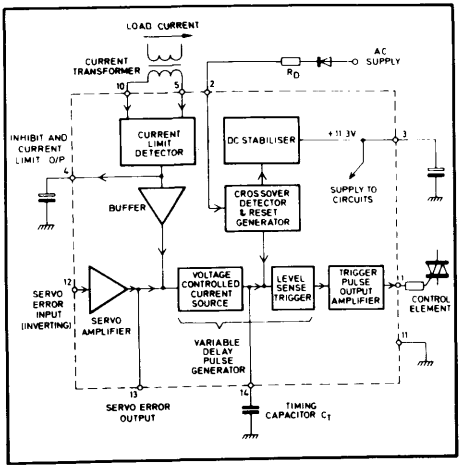


Fig.2 SL440 functional block diagram

ELECTRICAL CHARACTERISTICS @ T_{amb} = +25°C

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Firing pulse width		50		μs	
Max. pulse current	60	120		mA	
Current to pin 3	15		30	mA	Rectified AC
Voltage at pin 3 (internally stabilised)		11.3		+V	
Inhibit operating voltage (pin 4)	0		5	+V	
Static gain of servo amplifier		75		–	Typical application, gain = $\frac{R_L}{2k}$
Current limit input threshold		±0.7		V	

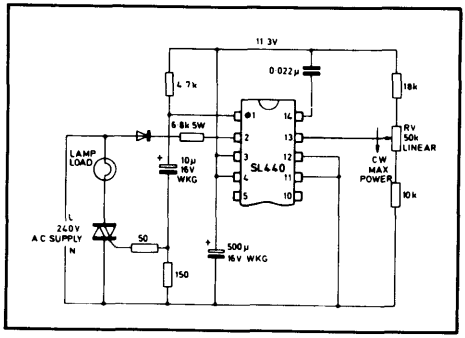


Fig.3 Lamp dimmer using minimum components

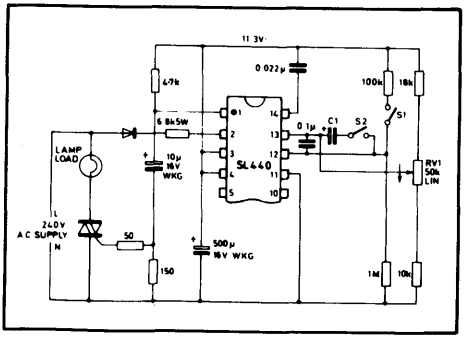


Fig.4 Automatic lamp fading circuit

APPLICATION NOTES

A simple, manually-controlled, lamp dimmer circuit is shown in Fig.3. In this application, the servo amplifier is not used; proportional control of lamp brightness is effected by the voltage applied via RV1 to the servo amplifier output (pin 13) which is internally connected to the conduction control circuit.

A more sophisticated use of the SL440 is shown in Fig.4 an automatic lamp fading circuit which has applications in a variety of domestic environments. The circuit is used as follows: with S1 and S2 both open, the level of brightness is directly controlled by the setting of RV1. When S1 is closed, the positive voltage applied to pin 12 causes firing pulses to be produced at a conduction angle approaching 180° (fig.5) and the lamp brightness is maximum. When S2 is closed and S1 is opened, the servo amplifier acts as an integrator due to the Miller action of C1 and the lamp brightness fades progressively to the level previously set by RV1. The fade rate is determined by the choice of C1: for example, a 250 microfarad capacitor will result in a subjectively imperceptible fade rate of 20-30 minutes.

Fig.6 shows the SL440 used in a motor speed control circuit. The DC motor/tacho-generator is used in a velocity servo loop in which motor velocity is linearly proportional to the setting of RV1. RV2 controls the maximum motor current in the range 1 to 10A.

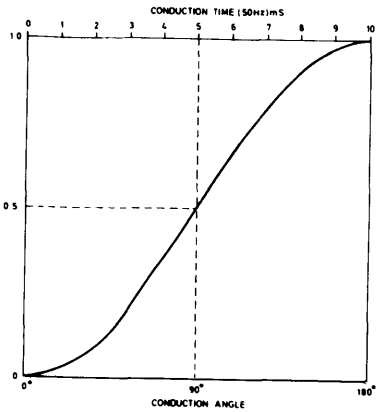


Fig.5 Triac conduction angle v. sinewave load power

OPERATING NOTES

In applications where RF radiation is a problem, it is recommended that the filter circuit shown in Fig.7 be used.

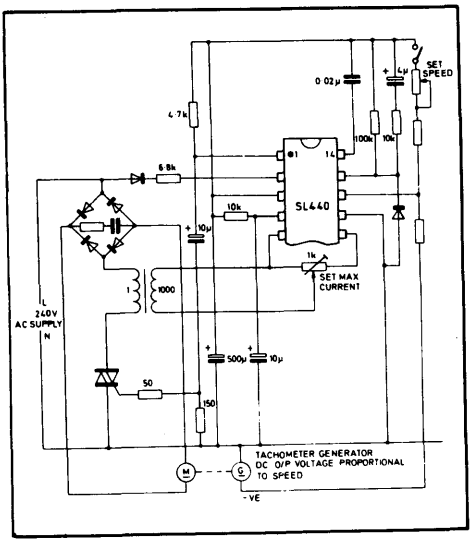


Fig.6 Servomotor control with motor current limiting

Where the SL440 is used for domestic light dimming, or in other applications where the power dissipated in the dropping resistor R_D is considered excessive, the series rectifier and dropping resistor can be replaced by the circuit shown in Fig.8. The series capacitor, together with the low impedance at pin 3, provides a degree of RF filtering at the AC supply terminals.

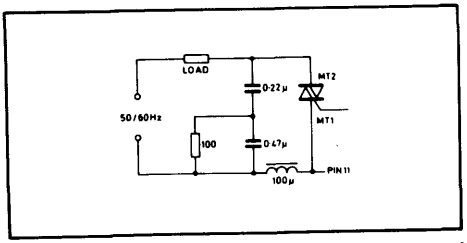


Fig. 7 RF filter for loads less than 100W or inductive. For loads of 100W and above, use 100µH and 0.1µF only.

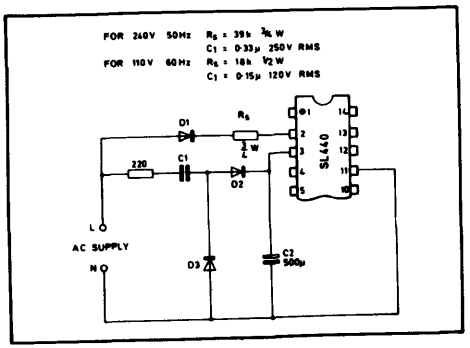


Fig.8 Low loss power supply

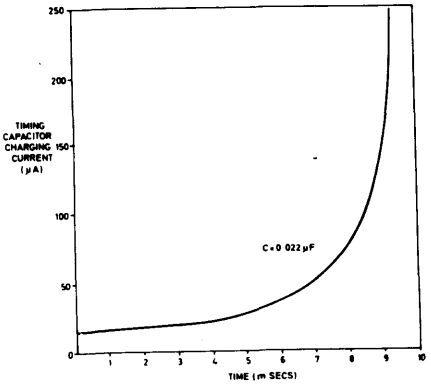


Fig.9 Triac conduction time v. capacitor charging current

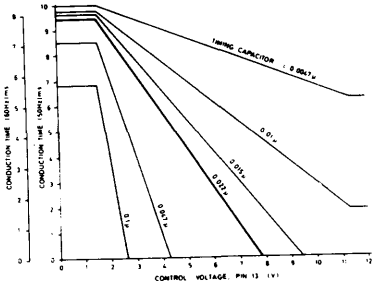


Fig.10 Triac conduction time v. servo amplifier output (demonstrating linear relationship)

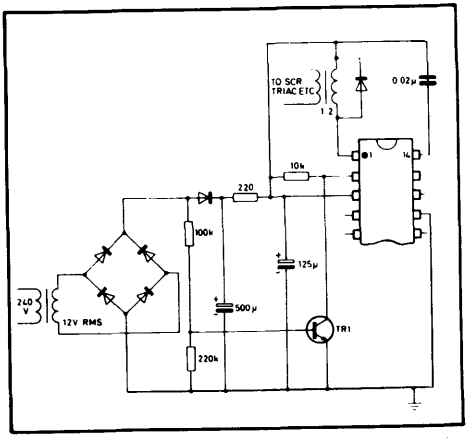


Fig.11 Fully isolated supply operation of SL440, featuring full-wave crossover detection for symmetrical timing. Additional SL440s can be powered via separate 220Ω feed resistors, synchronizing being achieved by connecting pin 2 of each SL440 to the collector of the common sync. transistor TR1.

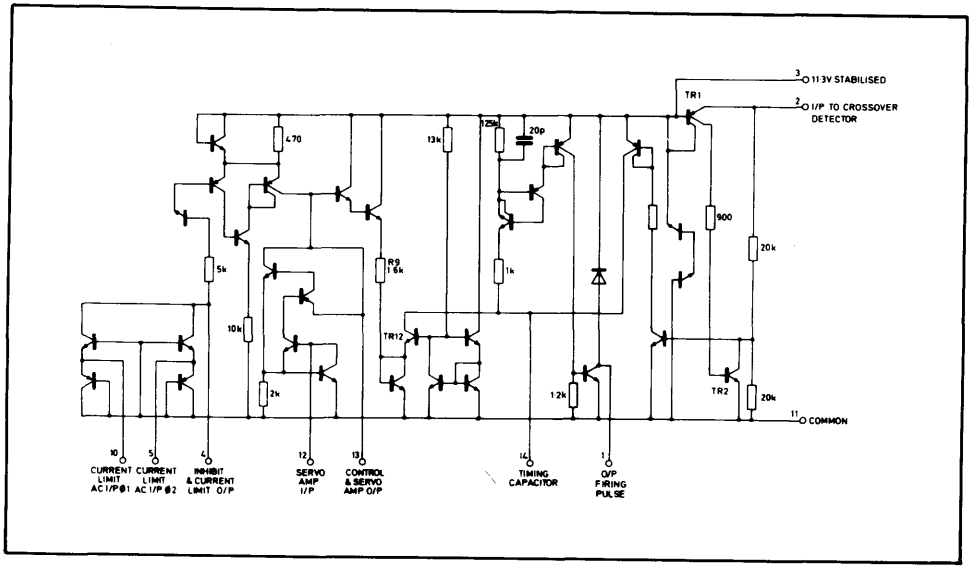


Fig.12 Circuit diagram of SL440

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +125°C
Operating temperature	−10°C to +65°C
Package dissipation	600 mW
Supply current to pin 2	200mA DC

NOTE

Where the SL440 is to be used in a device socket, care should be taken to ensure that the reservoir capacitor on pin 3 is discharged before inserting the device. Failure to observe this precaution may result in damage to the internal shunt stabiliser.

PLESSEY
Semiconductors

SL441A
ZERO VOLTAGE SWITCH

The SL441A is a symmetrical burst control integrated circuit in an 8 pin DIL package. When used with a triac, AC power may be regulated by varying the number of mains cycles applied to the load in a fixed timing period. The device is particularly suitable for temperature control applications including hairdryers, food warmers, soldering irons etc. Zero Voltage Switching has the advantage of minimising radio frequency interference.

SPECIAL FEATURES

1. Balanced zero voltage point crossing detector, spike filter and pulse generator for reliable triggering of the triac.
2. A period pulse generator and bistable which are arranged to provide symmetrical burst control and eliminate $\frac{1}{2}$ wave firing. (EN50.006, BS5406, 1976)
3. A ramp generator whose output is used to modify an internal reference voltage which is then compared with the voltage appearing on the thermistor to form a proportional control system. The period of the ramp generator is defined externally and may be chosen to limit 'lamp flicker' in accordance with EN50.006/ BS5406, 1976.
4. The comparison amplifier has inbuilt hysteresis to eliminate switching jitter and a spike filter/sampling circuit to provide high immunity to both spikes and coherent 50Hz/60Hz.
5. Thermistor malfunction may be sensed and power automatically removed.
6. A supply voltage sensing circuit which inhibits firing pulses when the supply is inadequate to guarantee proper circuit operation. This eliminates stressing of the triac at switch-on.

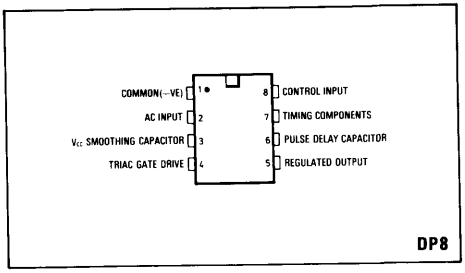


Fig. 1 Pin connections

ABSOLUTE MAXIMUM RATINGS

Voltages
Voltage on pin 8 V_{8-1} Max. 12V
Voltage on pin 4 V_{4-1} Max. 10V

Currents
Supply current (pin 2) Peak value $\pm I_{2M}$ 50mA.
Non-repetitive peak current (tp $\leqslant$250μs) $\pm I_{2SM}$ 200mA.
Output current (pin 5) Max. 5mA Short circuit protected.
Output current (pin 4) average value $I_{4(AV)}$ Max 5mA Short circuit protected.

Temperature
Operating ambient temperature T_{AMB} −10°C to +75°C
Storage temperature T_{STG} −30°C to +125°C

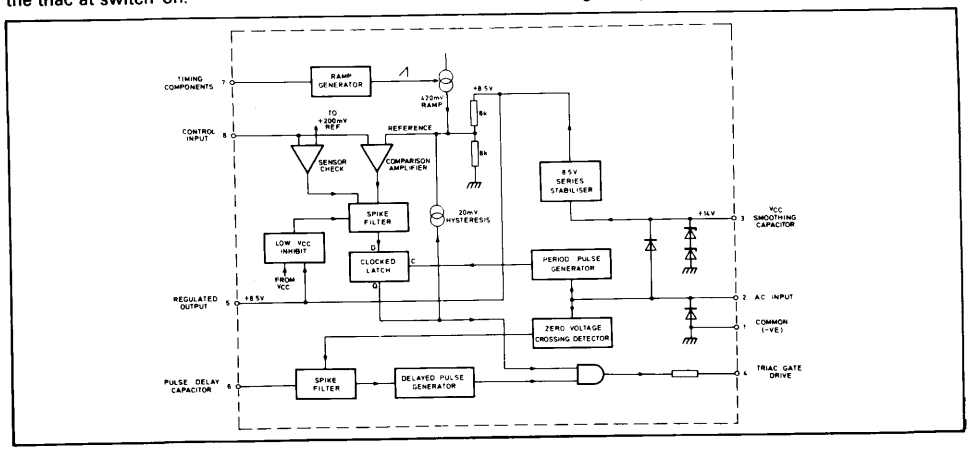


Fig. 2 Block schematic of SL441A

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{AMB} = 25°C
All voltages measured with respect to common (pin 1)

Characteristics	Value			Units
	Min.	Typ.	Max.	
Shunt regulating voltage pin 3 @ 16mA		14.7		V
Shunt regulating voltage pin 3 @ 16mA @ 75°C			16	V
Supply voltage trip level pin 3		12.2		V
Supply current (less I_4AV, I_5) (see Note 1)			7.5	mA
Regulated voltage pin 5	8.0	8.5	9.0	V
Regulated voltage temperature coefficient pin 5	−1		+1	mV/°C
Triac gate drive pin 4 (See Note 2)				
Open circuit ON voltage		8.5		V
Open circuit OFF voltage			0.1	V
Output current into 2V drain	100	130		mA
Output current into 4V drain	65	80		mA
Output current into short circuit			200	mA
Internal drain resistance		800		Ω
Control input pin 8				
Bias current			1	µA
Hysteresis		20		mV
Sensor malfunction circuit operates at	150	200	250	mV
Input working voltage range	0		12	V
Internal reference voltage (Ramp start) } (See Note 3)	4.0	4.25	4.5	V
Internal reference voltage (Ramp finish) }		4.67		V
Peak-to-peak amplitude of ramp	360	420	480	mV
Pin 6 output impedance (R6) (See Note 2)	21.5	27	32.5	kΩ
Maximum ripple voltage pin 3			1	V_{P-P}

NOTES
1. The supply current is 0.45 × (RMS current fed into pin 2). I_5 is the current drained from pin 5 externally. I_{4AV} is the average triac gate current supplied each mains cycle.
2. Triac firing pulse. t_p Pulse width 0.69 $R6C_D$µs typical
   t_f Pulse finish 1.09 $R6C_D$ µs minimum after zero voltage point R6 in kΩ, C_D in nF See Application circuit
   t_p Nominal (C_D = 2.7nF) = 50µs
   t_f Minimum (C_D = 2.7nF) = 63µs
3. Ramp period = 0.85 ±0.15 × R_TC_T sec. See Application circuit. The actual value of R_t must lie between 500kΩ and 3MΩ.

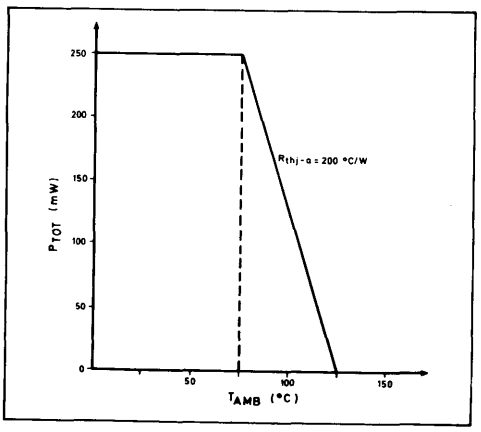


Fig. 3 Power dissipation

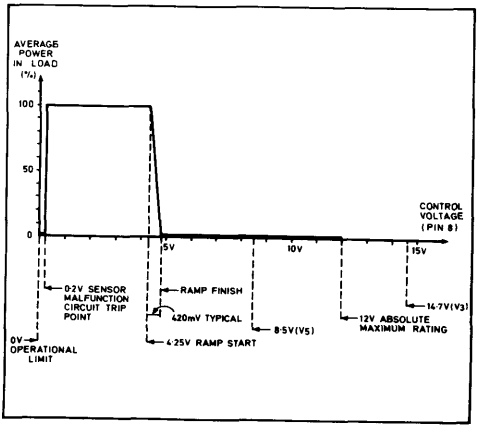


Fig. 4 Control characteristic

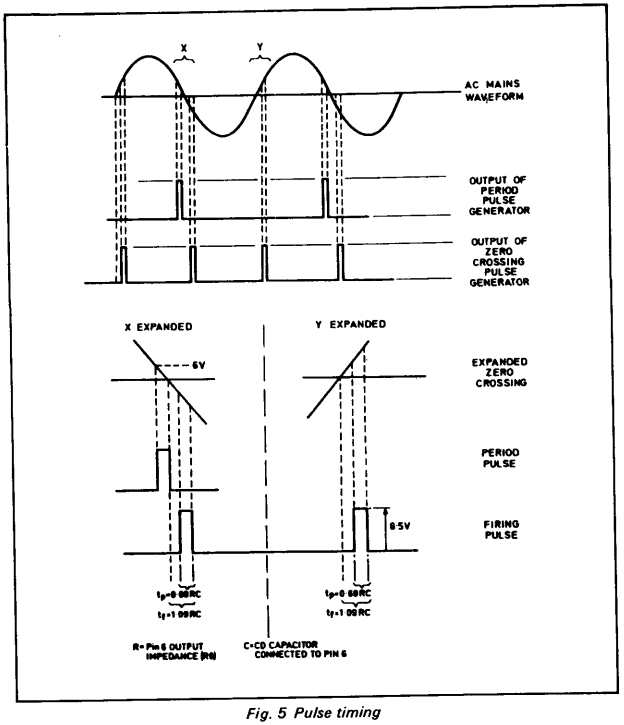
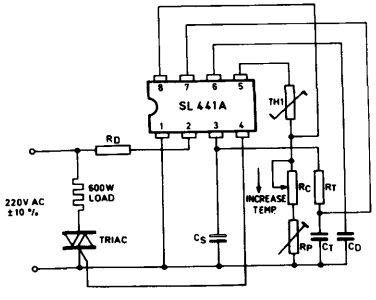


Fig. 5 Pulse timing

APPLICATIONS

Setting up

With R_C at zero resistance, adjust R_P to give the maximum output air temperature desired (eg 80°C). The value of R_C will determine the minimum regulated output air temperature (eg 40°C).



SUGGESTED VALUES

R_D	8.2kΩ 5% 6W (less in air stream)
R_C	22kΩ linear control potentiometer
R_P	10kΩ Preset
TH 1	NTC type R_{25} = 47k±20%; B≙4000°k eg GM473, VA3410 etc.
R_T	2.2M Ω } Ramp period = 0.4 sec.
C_T	0.22μF }
C_S	150μF 16V
C_D	2.2nF ±10%
Triac	TAG 225–400

Fig. 6 Application circuit for temperature regulated hairdryer

PLESSEY
Semiconductors

SL441C
ZERO VOLTAGE SWITCH

The SL441C is a symmetrical burst control integrated circuit in an 8 pin DIL package. When used with a triac, AC power may be regulated by varying the number of mains cycles applied to the load in a fixed timing period. The device is especially suited to room temperature control applications including panel heaters, fan heaters etc. Zero Voltage Switching has the advantage of minimising radio frequency interference.

SPECIAL FEATURES

1. Balanced zero voltage point crossing detector, spike filter and pulse generator for reliable triggering of the triac.
2. A period pulse generator and bistable which are arranged to provide symmetrical burst control and eliminate $\frac{1}{2}$ wave firing. (EN50.006, BS5406, 1976)
3. A ramp generator whose output is used to modify an internal reference voltage which is then compared with the voltage appearing on the thermistor to form a proportional control system. The period of the ramp generator is defined externally and may be chosen to limit 'lamp flicker' in accordance with EN50.006/ BS5406, 1976.
4. The comparison amplifier has inbuilt hysteresis to eliminate switching jitter and a spike filter/sampling circuit to provide high immunity to both spikes and coherent 50Hz/60Hz.
5. Thermistor malfunction may be sensed and power automatically removed.
6. A supply voltage sensing circuit which inhibits firing pulses when the supply is inadequate to guarantee proper circuit operation. This eliminates stressing of the triac at switch-on.

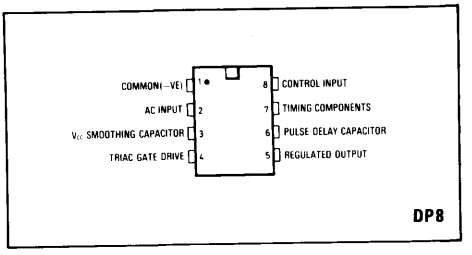


Fig. 1 Pin connections

ABSOLUTE MAXIMUM RATINGS

Voltages
Voltage on pin 8 V_{8-1} Max. 12V
Voltage on pin 4 V_{4-1} Max. 10V

Currents
Supply current (pin 2) Peak value : I_{2M} 50mA.
Non-repetitive peak current (tp $\leqslant$250μs) : I_{2SM} 200mA.
Output current (pin 5) Max. 5mA Short circuit protected.
Output current (pin 4) average value I_4(AV) Max 5mA Short circuit protected.

Temperature
Operating ambient temperature T_{AMB} —10°C to +75°C
Storage temperature T_{STG} —30°C to +125°C

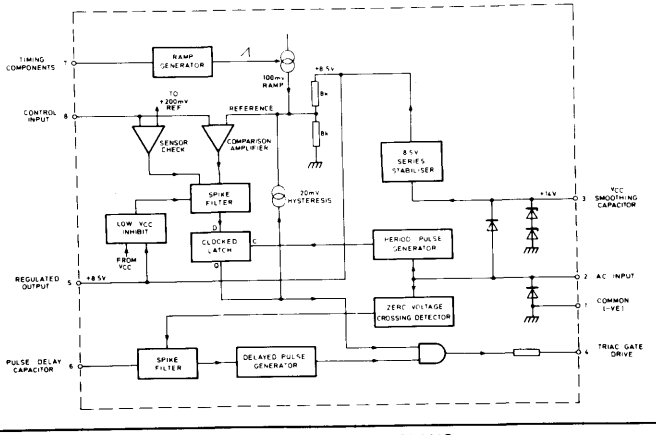


Fig. 2 Block schematic of SL441C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{AMB} = 25°C
All voltages measured with respect to common (pin 1)

Characteristics	Value			Units
	Min.	Typ.	Max.	
Shunt regulating voltage pin 3 @ 16mA		14.7		V
Shunt regulating voltage pin 3 @ 16mA @ 75°C			16	V
Supply voltage trip level pin 3		12.2		V
Supply current (less I_4AV, I_5) (see Note 1)			7.5	mA
Regulated voltage pin 5	8.0	8.5	9.0	V
Regulated voltage temperature coefficient pin 5	−1		+1	mV/°C
Triac gate drive pin 4 (See Note 2)				
Open circuit ON voltage		8.5		V
Open circuit OFF voltage			0.1	V
Output current into 2V drain	100	130		mA
Output current into 4V drain	65	80		mA
Output current into short circuit			200	mA
Internal drain resistance		800		Ω
Control input pin 8				
Bias current			1	µA
Hysteresis		20		mV
Sensor malfunction circuit operates at	150	200	250	mV
Input working voltage range	0		12	V
Internal reference voltage (Ramp start) (See Note 3)	4.0	4.25	4.5	V
Internal reference voltage (Ramp finish) (See Note 3)		4.35		V
Peak-to-peak amplitude of ramp	70	100	130	mV
Pin 6 output impedance (R6) (See Note 2)	21.5	27	32.5	kΩ
Maximum ripple voltage pin 3			1	V_{P-P}

NOTES
1. The supply current is 0.45 × (RMS current fed into pin 2). I_5 is the current drained from pin 5 externally. I_{4AV} is the average triac gate current supplied each mains cycle.
2. Triac firing pulse. t_p Pulse width 0.69 $R6C_D$µs typical
   t_f Pulse finish 1.09 $R6C_D$ µs minimum after zero voltage point R6 in kΩ, C_D in nF See Application circuit
   t_p Nominal (C_D = 2.7nF) = 50µs
   t_f Minimum (C_D = 2.7nF) = 63µs
3. Ramp period 0.85 ±0.15 × R_TC_T sec. See Application circuit. The actual value of R_t must lie between 500kΩ and 3MΩ.

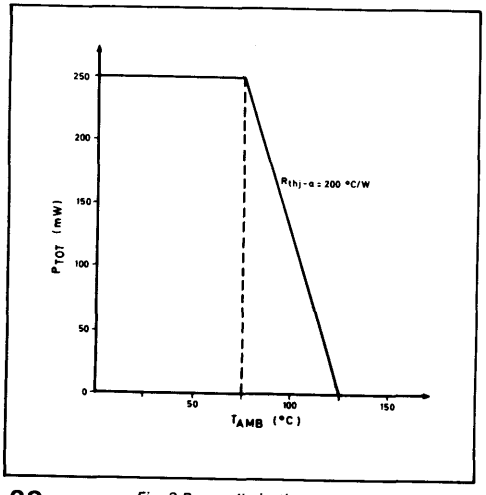


Fig. 3 Power dissipation

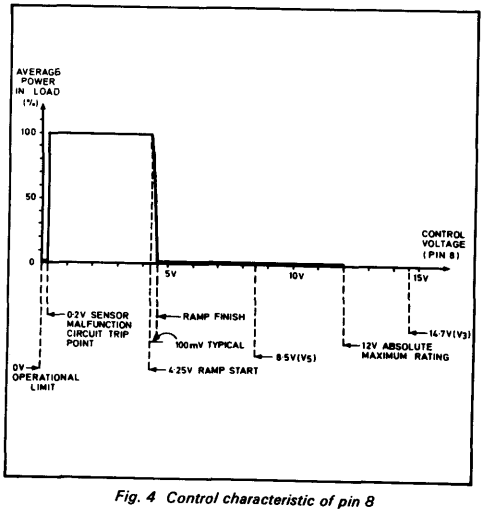


Fig. 4 Control characteristic of pin 8

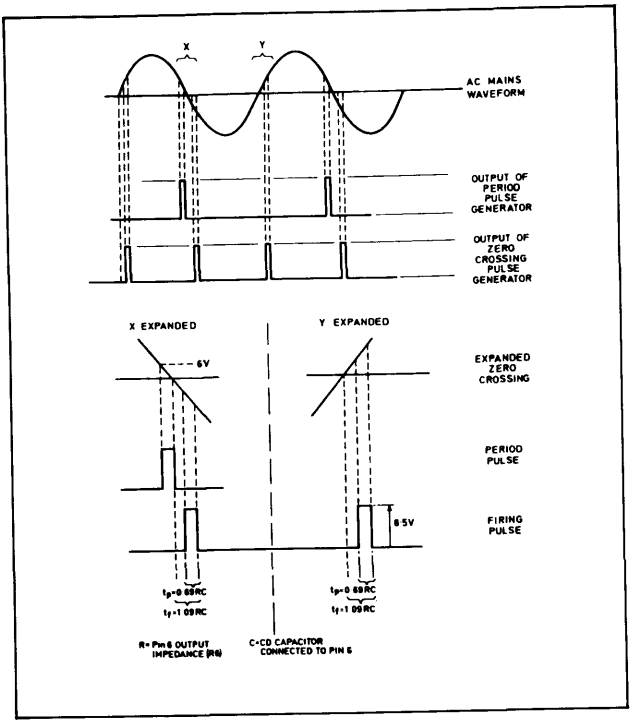
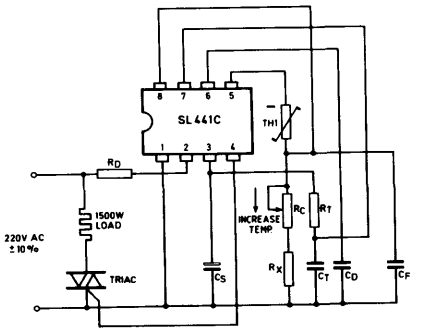


Fig. 5 Pulse timing

APPLICATIONS

Electronic thermostat for room heater

The circuit in Fig. 6 has a sensitivity of nominally 100mV/°C. The width of the proportional control band is nominally 1.0°C and offers a good compromise between temperature stability and regulation performance. For potentiometer control characteristics see Figs. 7 and 8.



SUGGESTED VALUES

R_D	8.2kΩ 5% 6W (less in air stream)	
R_C	22kΩ linear control potentiometer	
R_t	2.7MΩ	} Ramp period = 11 secs.*
C_t	4.7µF 10V TANT	
C_f	47nF (filter if required)	
C_S	150µF 16V	
C_D	2.2nF ±10%	
Triac	TAG 250-400	

TH1 NTC thermistor. R_{25} = 10kΩ
B = 4200. e.g. ITT KQ103

R_x 6.2k ±5% fixed resistor or 10kΩ preset.
See control characteristics Figs. 7 and 8

*If on-off control is required, omit R_T and C_T and link pin 7 to pin 1.

*Fig. 6 Application circuit for proportional temperature control system.**

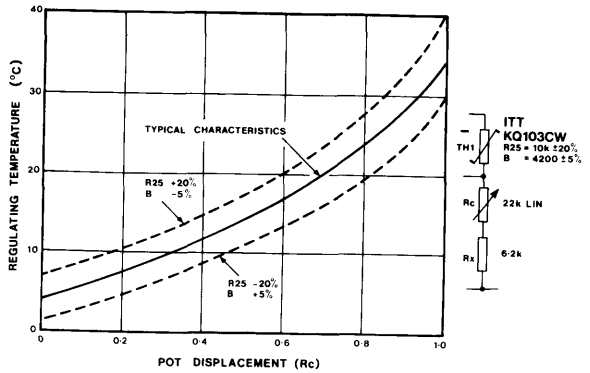


Fig. 7 Control characteristics of electronic room thermostat (mechanical calibration)

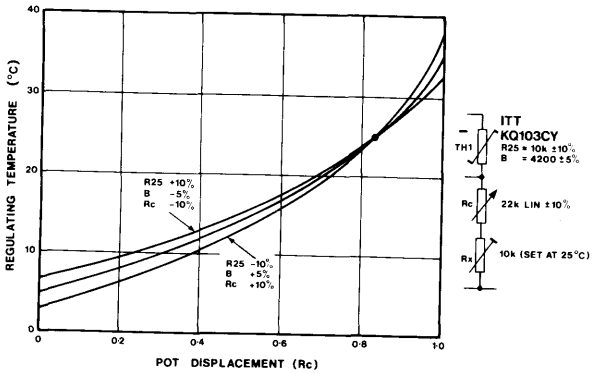


Fig. 8 Control characteristics of electronic room thermostat (electrical calibration)

PLESSEY
Semiconductors

SL443A

ZERO VOLTAGE SWITCH

The SL443A is a symmetrical burst control integrated circuit in an 8-pin DIL plastic package and is mainly intended for manual heat control applications, for example cooker hot plates and powerful hair dryers.

SPECIAL FEATURES

1. Well defined load power/potentiometer displacement characteristics
2. High immunity against spurious triac firing under noisy mains environment (automatic spike filtration)
3. Enables compliance with Cenelec EN50,006/ BS5406-1976
   (A) Switching rate controlled
   (B) symmetrical burst control
4. Very low external component count
5. Triac firing pulses inhibited whilst the ICIs power supply is being established.

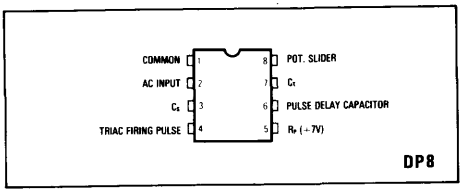


Fig. 1 Pin connections (top)

APPLICATIONS

- Cooker hotplates
- Powerful hairdryers

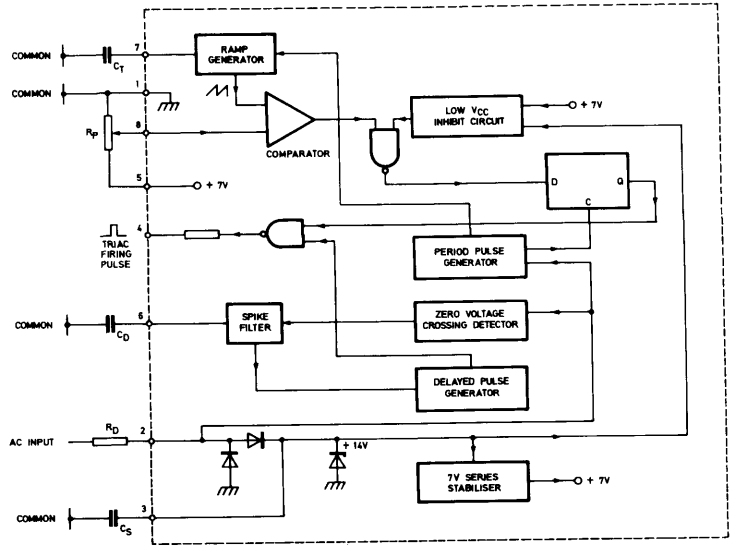


Fig. 2 SL443A block diagram

CIRCUIT DESCRIPTION

The externally current limited AC supply is applied to the device, and rectification followed by shunt regulation provides a 14V DC supply. This is externally smoothed before application to the 7.0V series stabiliser which feeds the resistance bridge. The stabiliser must be within regulation, or operation of the 'Low Vcc Inhibit' circuitry and prevents unsuitable firing pulses from being supplied to the triac at 'switch-on'. The current limited AC supply also drives the Period Pulse Generator (PPG) and zero voltage crossing circuits.

The PPG produces a single short duration pulse for each completed mains cycle and serves two purposes. Firstly it is used to clock logic information such that the circuit behaves in a symmetrical manner and only complete mains cycles are applied to the load. Secondly the pulse is used to switch timing components in the ramp generator and this enables long time constants to be achieved without having to resort to the use of electrolytic capacitors.

The zero voltage crossing detector controls a pulse generator that has a delayed output. The delay is necessary since, with loads that are slightly inductive or low power resistive, the triac load current may not reach its required holding level at zero voltage point.

Both delay and pulse duration are defined by an external capacitor and this further serves the purpose of filtering out spikes which occur in the zero crossing region. Automatic rejection takes place of spikes having a duration of up to 50 per cent of the normal width of the triac firing pulse.

The comparator amplifier has differential inputs and these are used to compare the potential appearing on the slider of the control potentiometer with that of the ramp waveform. The output of this amplifier controls the logic circuitry and the potentiometer setting defines the fraction of the ramp period for which the triac is in conduction so controlling the power in the load.

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)
T_{AMB} = 25°C,
All voltages measured with respect to common (pin 1)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Shunt regulating voltage pin 3		14.7		V	I_3 = 16mA
Shunt regulating voltage pin 3			16	V	I_3 = 16mA, T_{amb} = +75°C
Supply voltage trip level pin 3		12.2		V	
•Supply current (less I_4 AV, $2 \times I_5$) See Note 1			7.2	mA	
Potentiometer supply pin 5, V_5	6.8	7.0	7.6	V	
Potentiometer resistance range	18		140	kΩ	
Triac gate drive pin 4					
Open circuit ON voltage		8.5		V	
Open circuit OFF voltage			0.1	V	
Output current into 2V drain	80	100		mA	
Output current into 4V drain	50	70		mA	
Output current into short circuit			200	mA	
Internal drain resistance		800		Ω	
Control input pin 8					
Bias current			1	μA	
Internal reference – ramp start	0.3	0.5	0.7		
– ramp finish	V_5– 0.5	V_5–0.3	V_5– 0.1		
★ Period of ramp generator – T	27	30	33	s	(R_P = 100K, C_t = 0.68μ) (RMS mains voltage=220v)
Pin 6 output impedance R6	21.5	27	32.5	kΩ	

• The supply current is 0.45 x (RMS current fed into Pin 2)

★ Period of ramp = T = $2 \times C_T \times R_P \times$ (RMS mains voltage) seconds

ABSOLUTE MAXIMUM RATINGS

Voltages

Voltage on pin 8,	V_{8-1}	Max	10v
Voltage on pin 4,	V_{4-1}	Max	10v

Currents

Supply current, pin 2 peak value ± I_{2M}	Max	50mA
Non-repetitive peak current ($t_P \geqslant 250\mu S$) ± I_{2SM}	Max	200mA
Output current, pin 5 I_5	Short circuit protected	
Output current, pin 4, average value I_4 (AV)	Max	10mA
	Short circuit protected	

Temperatures

Operating ambient temperature	T_{AMB} —10 to 75°C
Storage temperature	T_{STG} —55 to +125°C
Power Dissipation	See Fig. 3

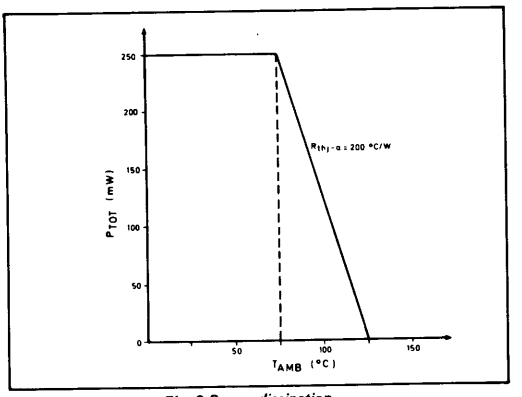


Fig. 3 Power dissipation

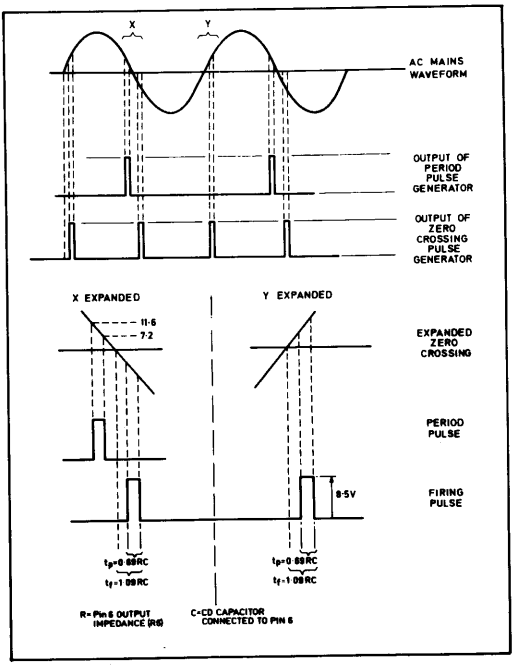


Fig. 4 Method of control

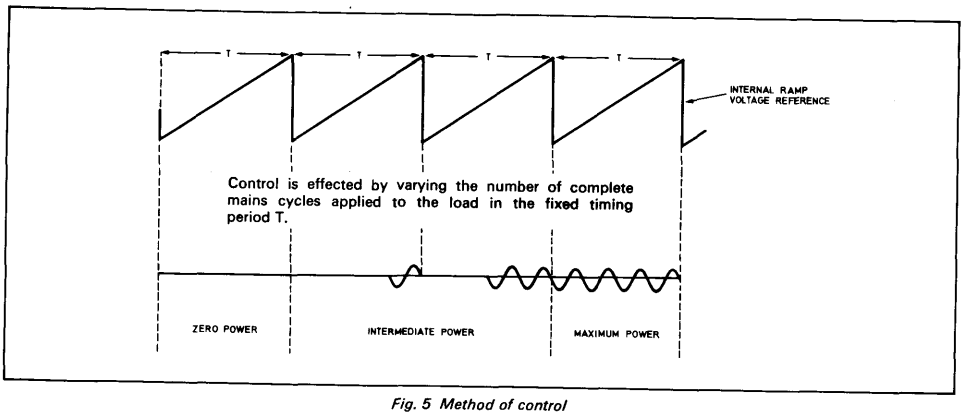
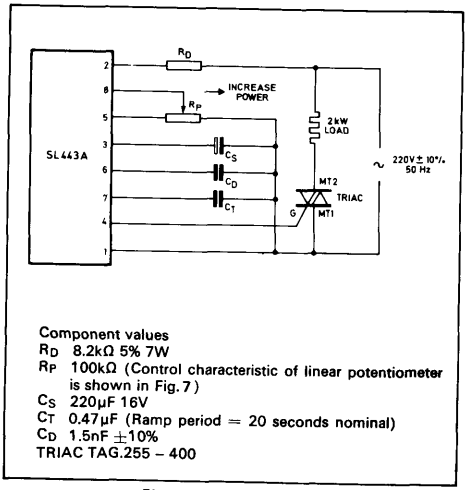
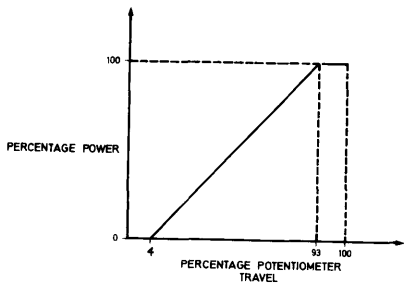


Fig. 5 Method of control



Component values
R_D 8.2kΩ 5% 7W
R_P 100kΩ (Control characteristic of linear potentiometer is shown in Fig. 7)
C_S 220μF 16V
C_T 0.47μF (Ramp period = 20 seconds nominal)
C_D 1.5nF ±10%
TRIAC TAG.255 – 400

Fig. 6 Cooker hotplate control



This characteristic applies to a linear potentiometer. Different control characteristics are easily obtained by using a non-linear potentiometer and/or offset resistors in the potentiometer circuit.

Fig. 7 Output power v. potentiometer displacement

PLESSEY
Semiconductors

SL445A

ZERO VOLTAGE SWITCH

The SL445 is a triac controller providing a *complete* solution for temperature controlled electric panel heaters, cookers, film processing baths etc.

Switching occurs at the zero voltage point in order to minimise radio frequency interference.

The device is suitable for mains-on-line operation and requires minimal external components.

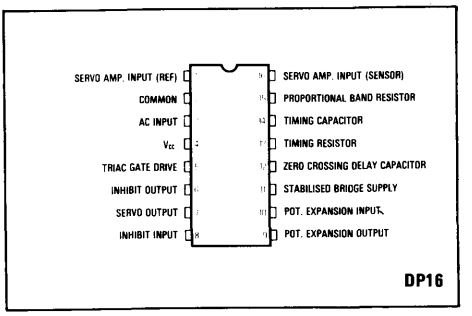


Fig. 1 Pin connections (top)

SPECIAL FEATURES

1. Choice of proportional or on/off temperature control.
2. Controlled switching rate in order to limit 'lamp flicker' (as per EN50,006). A pulse integration technique eliminates the problems associated with electrolytic timing capacitors.
3. Very accurate temperature control is possible since switching jitter has been eliminated *without introducing hysteresis* to the servo amplifier.
4. Symmetrical burst control i.e. no half-wave firing (as per EN50,006).
5. LED drive circuit which responds directly to the temperature setting.
6. Over-temperature protection circuit using a 'fail-safe' PTC thermistor and having the option of automatic or manual reset.
7. LED/Buzzer drive circuit controlled by 6 above.
8. High immunity against spurious triac trigger pulses under noisy mains environment.
9. Spurious triac trigger pulses inhibited at 'switch-on'.
10. Potentiometer expansion circuit to improve resolution/reduce component count.

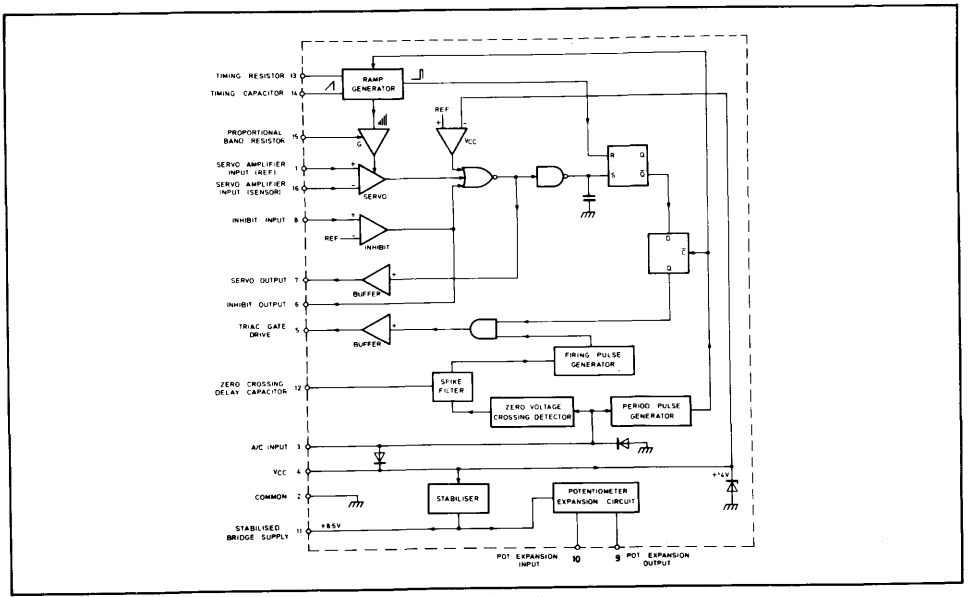


Fig. 2 SL445 block diagram

CIRCUIT DESCRIPTION

The externally current limited AC supply is applied to the device and rectification followed by shunt regulation produces a 14V DC supply.

This is externally smoothed before application to the 8.5V series stabiliser which must be within regulation or operation of the 'Low Vcc Inhibit' circuit will result. This latter circuit overrides all other circuitry and prevents unsuitable firing pulses from being supplied to the triac at 'switch-on'. The current limited AC supply also drives the Period Pulse Generator (PPG) and Zero Voltage Crossing circuits.

The PPG produces a single short duration pulse for each completed mains cycle and serves two purposes. Firstly it is used to clock logic information such that the circuit behaves in a symmetrical manner and only complete mains cycles are applied to the load. Secondly the pulse is used to switch timing components in the ramp generator and this enables long time constants to be achieved without having to resort to the use of electrolytic capacitors.

The Zero Voltage Crossing Detector controls a pulse generator that has a delayed output. This delay is necessary since with loads that are slightly inductive or low power resistive, the triac load current may not reach its required holding level at the zero voltage point.

Both delay and pulse duration are defined by an external capacitor and this further serves the purpose of filtering out spikes which occur in the zero crossing region. Automatic rejection takes place of spikes having a duration of up to 50 per cent of the normal width of the triac firing pulse.

The Servo Amplifier has differential inputs and these are used to sense the output of the bridge containing the room temperature sensing thermistor. The output of this amplifier is NOR-gated with the outputs of the Inhibit Amplifier and the Low Vcc Amplifier.

The output of this gate is accessible such that it may be used to control an LED so indicating whether or not the appliance is consuming electricity .The output from the NOR gate is also applied to an active spike filter before application to the S input of the R/S Bistable. Since this bistable can only be reset once every ramp generator cycle, it follows that a definite limitation is imposed on the switching rate of the system and this enables compliance with the requirements of the EN50-006 regarding 'lamp-flicker'.

An externally defined proportion of the ramp waveform may be applied to the 'offset' of the Servo Amplifier such that the amplifier has an offset which varies linearly with time. This has the effect – as the bridge approaches balance – of varying the power output in proportion to the difference between the set temperature and the actual temperature i.e. Proportional Control. The advantage of this arrangement is that the approach of bridge balance is anticipated and overshoot is avoided.

The potentiometer expansion circuit matches the characteristics of a typical NTC thermistor to provide good resolution and linear temperature control over the normal domestic temperature range.

The Bridge is supplied with a stable 8.5V supply from the series stabiliser and one ninth of this supply is used as a reference voltage for the Inhibit Amplifier. This reference is compared with the voltage appearing across the PTC thermistor which is used to sense an overtemperature condition. The output of the Inhibit Amplifier is used to control the NOR gate which has already been mentioned and is also made accessible such that visual or audible warning may be provided. In addition, a suitable resistor may be connected between amplifier input and output to provide hysteresis should this be required. Choice of resistor value will determine whether the circuit works in an automatic or manual reset mode.

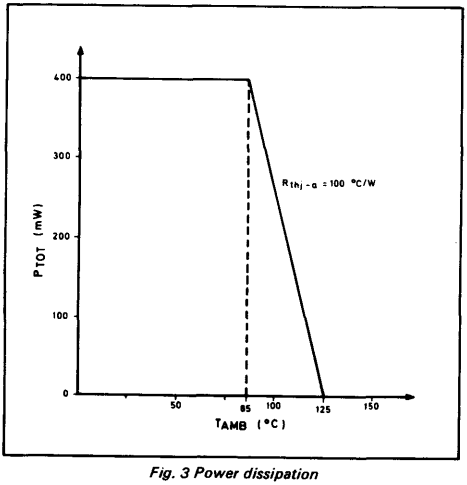


Fig. 3 Power dissipation

ABSOLUTE MAXIMUM RATINGS

Pin	Max.	Units
1. Applied voltage	V_4	V
3. Peak Repetitive Current in ($\pm I_{2M}$)	80	mA
3. Non-repetitive peak current (tp <250μS) $\pm I_{2SM}$	200	mA
5. Applied voltage	10	V
6. Applied Voltage	10	V
6. Output Current	10	mA
7. Applied Voltage	6	V
7. Output Current	10	mA
8. Applied Voltage	10	V
9. Applied Voltage	V_{11}	V
10. Applied Voltage	V_{11}	V
11. Output Current	10	mA
16. Applied Voltage	V_4	V

ELECTRICAL CHARACTERISTICS

Operating temperature range −10°C to + 85°C
Storage temperature range −55°C to +125°C

Test conditions (unless otherwise stated):
T_{amb} = 25°C
All potentials measured with respect to common (pin 2)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Shunt regulating voltage Pin 4		14.7		V	I_4 = 20mA average
Max. regulating voltage on Pin 4 at 85°C			16	V	I_4 = 20mA average
Supply sensing amplifier – minimum working voltage Pin 4		12.2		V	
Quiescent current drain *			8.2	mA	Less I_{11}, I_7, I_6, I_{5AV}
Stabilised bridge supply voltage Pin 11 @ 2mA	8.0	8.5	9.0	V	
Temperature coefficient Pin 11	−1		+1	mV/°C	
Triac gate drive Pin 5					See Fig. 7 for pulse timing
Open circuit OFF voltage			0.1	V	
Open circuit ON voltage		8.5		V	
Current drive into short circuit			200	mA	
Current drive into 2V drain	80	100		mA	
Current drive into 4V drain	50	70		mA	
Internal drain resistance Pin 5		800		Ω	
Servo amp. Pins 1 & 16					
Input bias current			1	µA	
Input working voltage range	0		10	V	
Servo amp. output voltage drive Pin 7	6.0	6.5	7.0	V	
Internal drain resistance Pin 7	10	25	60	kΩ	
Inhibit amp. input Pin 8					
Trip voltage	0.9	0.95	1.0	V	$V_{11} \div 9$
Input bias current			1	µA	
Input working voltage range	0		10	V	
Inhibit amp. output voltage drive Pin 6	5.8	6.4	6.8	V	
Internal drain resistance Pin 6	8	12	16	kΩ	
Inhibit voltage Pin 6		3.5		V	
Potentiometer expansion circuit input bias current Pin 10			10	µA	See Fig. 8
Potentiometer expansion circuit output resistance Pin 9	4	6	8	kΩ	See Fig. 8
Proportional control band (R_{15} = 220k)	60	100	140	mV	R_{15} = 220kΩ
Ramp generator period T	40	44	48	s	R_{13} = 100k, R_{14} = 1.0µF, 220V AC

★ The supply current is 0.45 × (RMS current fed into Pin 3)

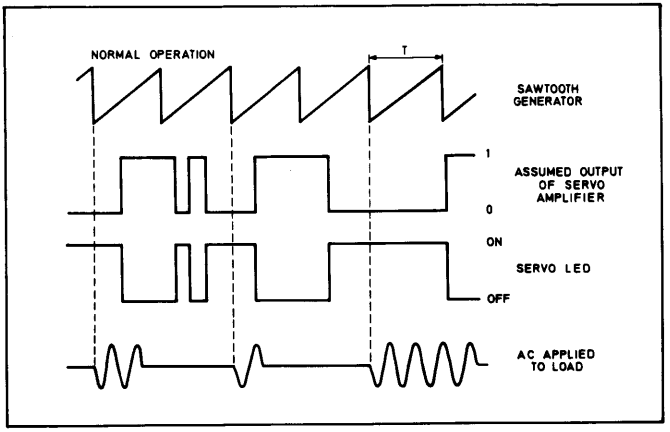


Fig. 4 Timed on/off control

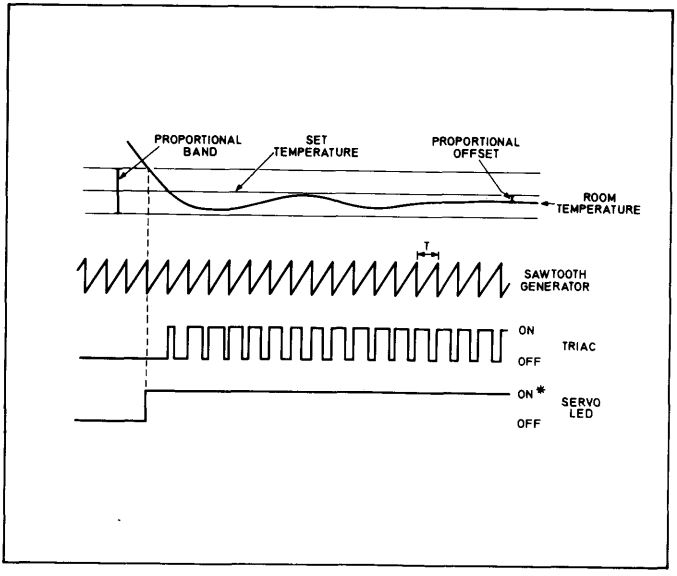


Fig. 5 Timed proportional control normal operation

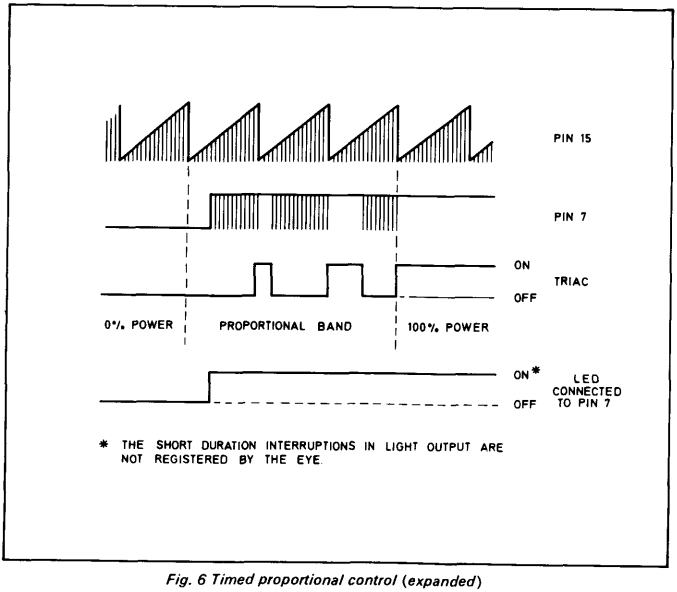


Fig. 6 Timed proportional control (expanded)

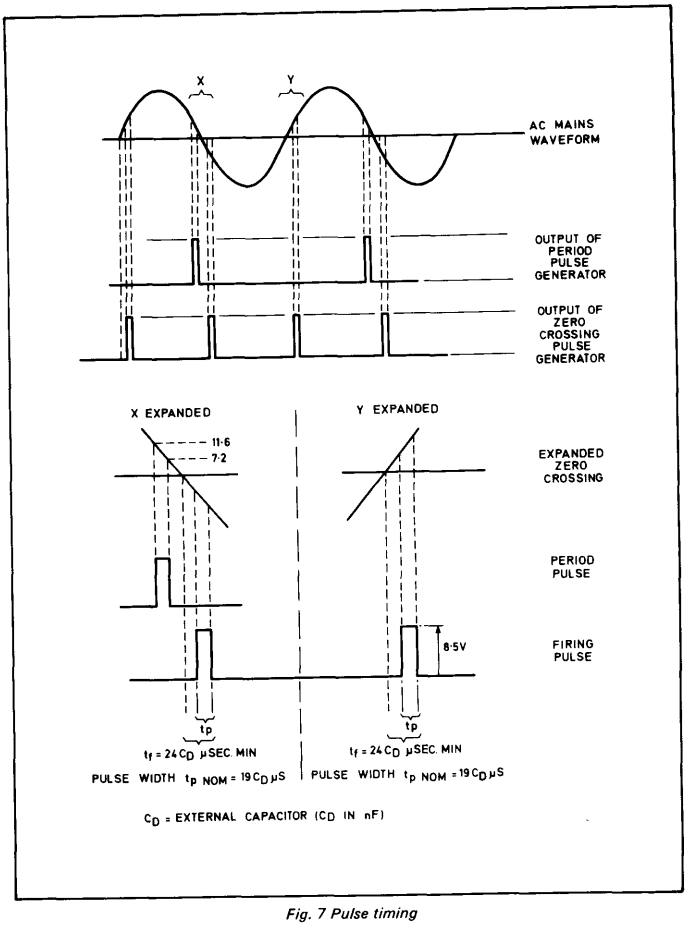


Fig. 7 Pulse timing

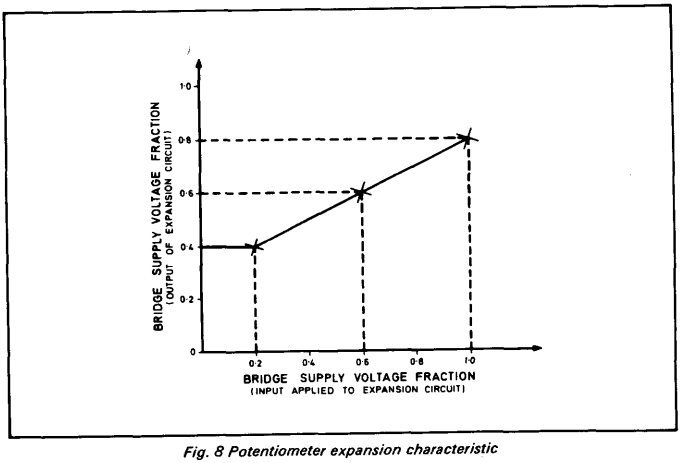
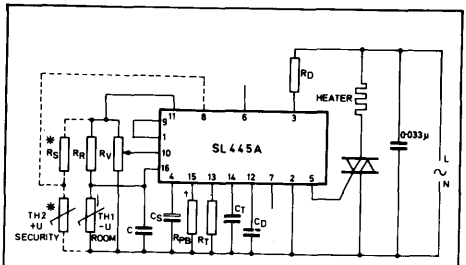


Fig. 8 Potentiometer expansion characteristic



* These two components may be omitted if the over-temperature trip facility is not required. Pin 8 should then be taken to common ie. Pin 2.

† This component may be omitted if proportional control is not required. The circuit will then provide time on/off control. Pin 15 should be taken to Pin 11.

C May be required to integrate input noise e.g. 47nF.

Fig. 9 Electric panel heater control with room thermostat and optional security thermostat

LED INDICATOR

Provides the following facilities

(a) In the case of timed proportional control, the LED will be lit continuously if any energy is supplied during the timing cycle, i.e. the LED will only be extinguished if the room temperature is being maintained without panel assistance.

(b) In the case of timed on/off control, the LED will be lit for the period that energy is being consumed, i.e. the LED will flash on and off as the room temperature varies about the set point.

(c) Room temperature may be ascertained by observing LED action whilst adjusting the temperature setting i.e. the LED is a substitute for the sound produced by electromechanical thermostats.

The LED facility may be added as shown in Fig. 10.

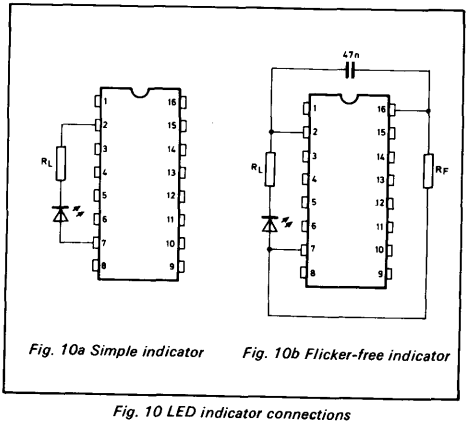


Fig. 10a Simple indicator *Fig. 10b Flicker-free indicator*

Fig. 10 LED indicator connections

It is desirable to minimise LED drive current since this has a significant effect on the power rating of the mains dropping resistor RD. If the LED is for facility 'a' or 'b', a high intensity, wide viewing angle LED will be required and a current of 5mA nominal is suggested i.e. $R_L = 1k\Omega$ ($V_{LED} = 1.5V$).

If the LED is only intended for facility 'c', a small, narrow viewing angle LED may be used and a current of 0.5mA nominal is sufficient i.e. $R_L = 10k\Omega$ ($V_{LED} = 1.5V$).

A small amount of positive feedback may be applied to the servo amplifier by inclusion of resistor Rf (Fig. 106). This can ensure flicker free operation of the LED by increasing the immunity of the amplifier to noise etc. on its input connections. However, the level of feedback should be minimised since temperature regulation will necessarily be impaired. A typical value for Rf would be 4.7 MΩ and this results in a hysteresis of 13mV (0.13°C) if the bridge components are as given below.

SECURITY (OVERTEMPERATURE TRIP) INDICATION

Indication may be provided by LED or buzzer as shown in Fig. 11.

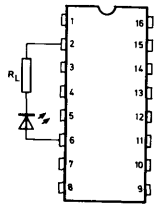


Fig. 11a LED ($I_{LED} = 5mA$, $V_L = 1.5V$, $R_L = 1k\Omega$; $I_{LED} = 0.5mA$, $V_L = 1.5V$, $R_L = 10k\Omega$)

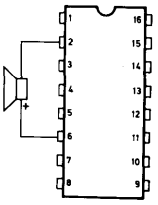
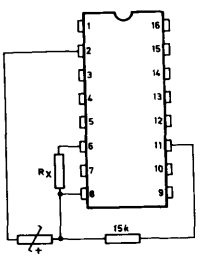


Fig. 11b Buzzer (6V, 6mA)

Fig. 11 Security indicator circuits

SECURITY (OVERTEMPERATURE TRIP) RESET

Hysteresis may be externally applied to the Inhibit Amplifier such that re-entry of the control circuit takes place automatically i.e. when the panel temperature falls to a certain level below the trip point. Alternatively, it may be arranged that the trip circuit – when activated – can only be reset by manual intervention e.g. momentarily interrupting the mains supply. It is desirable to introduce some hysteresis to the system when using a buzzer, in order to ensure positive on/off operation. When the manual reset mode of operation is adopted, an additional capacitor is required to eliminate the possibility of a spurious spike tripping the circuit.



Rx = 120k reset occurs 1°C below the trip point.
Rx = 56k reset occurs 2°C below the trip point.
(Above assumes that the PTC thermistor has a +15%/°C coefficient in the region of the trip temperature e.g. the ITT positte range.)

Fig. 12 Automatic reset

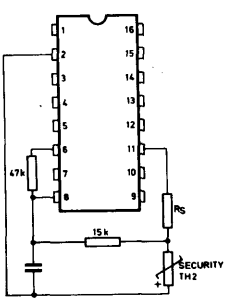


Fig. 13 Manual reset

COMPONENT VALUES

Room Temperature Sensing (R_R, TH1, Rv)

Rv = 22k or 25k linear control potentiometer.
R_R = 18k ±2%
THI = NTC thermistor, e.g. ITT type KQ223Y,
R_{25} = 22k ±10%, B = 4300 ±5%

Using these components, substantially linear temperature control is obtained over the range 5°C to 35°C. This range is covered by 69% of the potentiometer track when the I.C's expansion circuit is used as shown in figure I. If the LED facility is used, calibration can be both accurate and rapid.

Controlled Switching rate (R_T, C_T)

The period of the ramp generator is dictated by the requirements of Cenelec EN50.006 concerning lamp flicker. The load can only be switched into circuit at the start of a ramp cycle i.e. if power is interrupted to the load at any point in the cycle, subsequent demands for power can only be met at the start of the next cycle.

The pulse integration technique employed in the ramp generator accounts for the mains voltage term in the formula:

Period of ramp = $0.2 \times V_{RMS} \times C_T$ seconds ±10%

This assumes R_T = 100k. C_T is in µF, and V_{RMS} is in volts, e.g. a 1.0µF capacitor will provide a ramp period of 44 sec if the circuit is used with a 220V AC supply.

The capacitor should be of polyester or similar construction. Because of leakage and other considerations, electrolytic capacitors are not suitable.

Proportional Control (R_{PB})

Resistance R_{PB} controls the proportion of the ramp waveform which is applied internally to the offset facility of the servo amplifier. R_{PB} therefore, controls the width of the proportional control band.

If R_{PB} = 220k, the peak offset will be 100mV which is equivalent to a proportional control band of 1°C if the above bridge component values are used.

If R_{PB} = 100k, PB = 2.2°C
= 390k, PB = 0.55°C etc.

Overtemperature Control (Security) (Rs, TH2)

Rs = 15k

	Trip Temperature Min.	Max.
TH2 = ITT POSITTE PTC thermistor type YC080TB	82°C	90°C
= ITT POSITTE PTC thermistor type YC090TB	92°C	100°C
= ITT POSITTE PTC thermistor type YC100TB	102°C	110°C

Thermistors of alternative manufacture may be used although the value of Rs may then differ. Tripping takes place if the resistance of TH2 is greater than Rs ÷ 8.

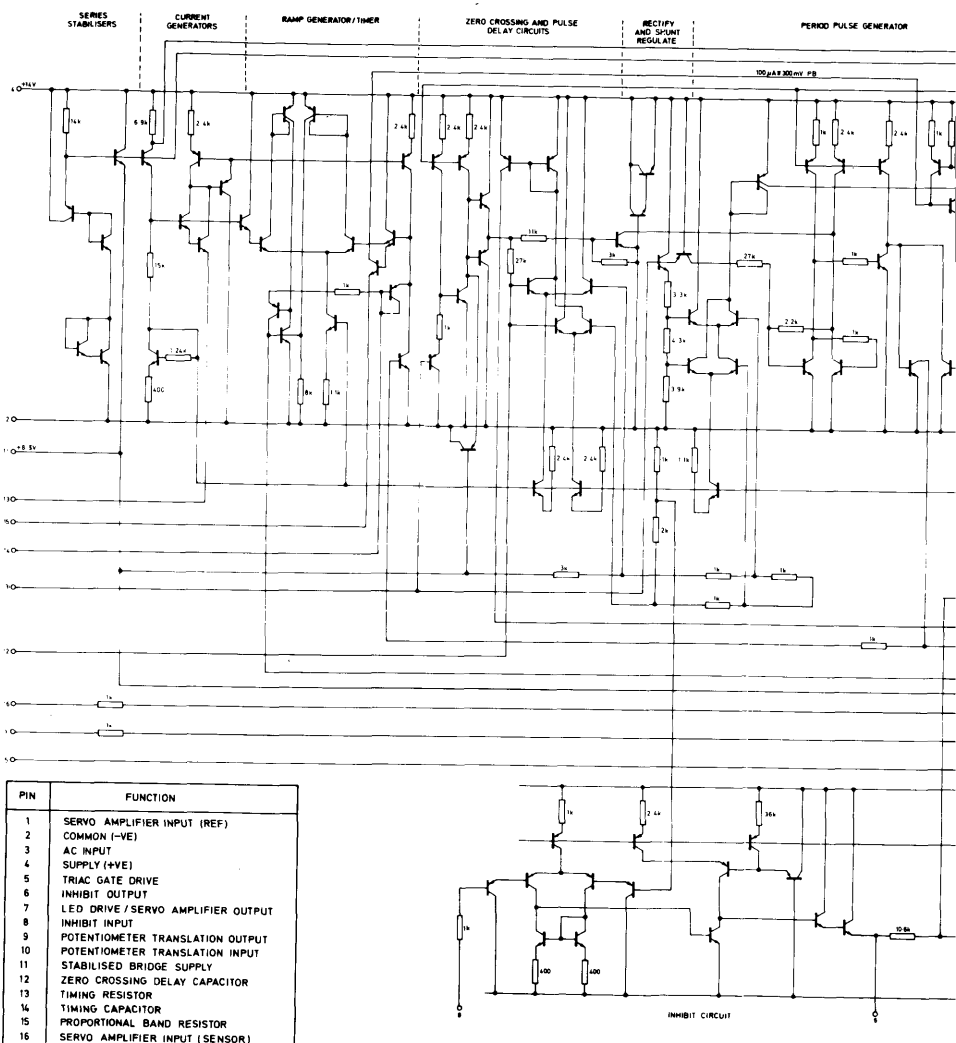
The value of Rs should be kept high to minimise power loss in R_D.

Triac and C_D

Generally, the maximum gate firing voltage (V_{GT}) of a triac is 2.0V and the output stage of the IC has been designed to deliver a minimum of 80mA into such a load. The nominal current is 100mA and the triac is supplied with positive gate current. A wide range of suitable, low price triacs are available from several manufacturers. In order to minimise RFI, a triac should be chosen which has a low latching current I_L. The triac cannot latch until the supply voltage $V_L \geq (V_T + I_L \times R_L)$ where
V_T = on-state voltage of the device
R_L = resistance of the triac load
Therefore the triac requires a gate current

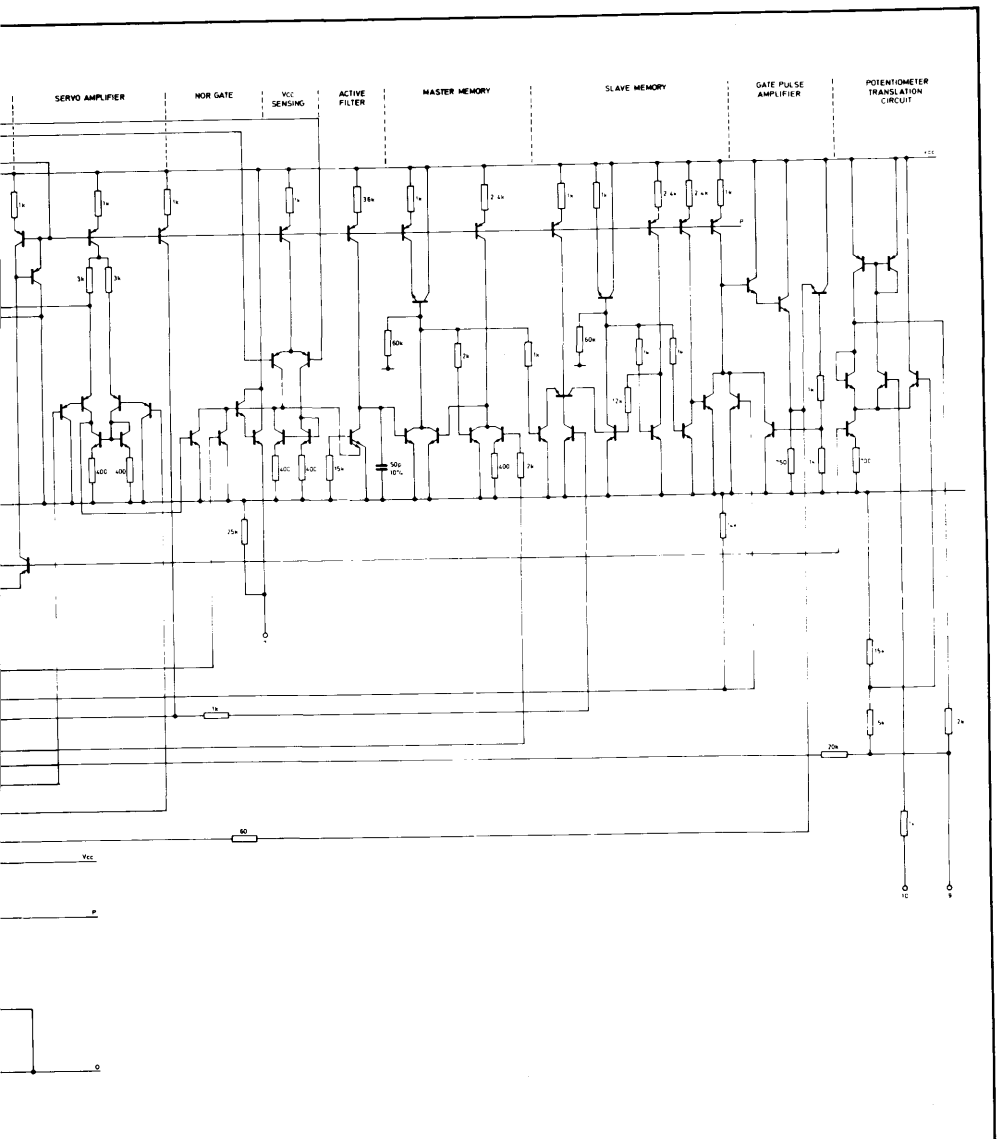
$$\frac{V_L \times 10^6}{V_{RMS} \times \sqrt{2} \times 2\pi f} \mu s$$

after the zero crossing point in the supply cycle where



PIN	FUNCTION
1	SERVO AMPLIFIER INPUT (REF)
2	COMMON (-VE)
3	AC INPUT
4	SUPPLY (+VE)
5	TRIAC GATE DRIVE
6	INHIBIT OUTPUT
7	LED DRIVE / SERVO AMPLIFIER OUTPUT
8	INHIBIT INPUT
9	POTENTIOMETER TRANSLATION OUTPUT
10	POTENTIOMETER TRANSLATION INPUT
11	STABILISED BRIDGE SUPPLY
12	ZERO CROSSING DELAY CAPACITOR
13	TIMING RESISTOR
14	TIMING CAPACITOR
15	PROPORTIONAL BAND RESISTOR
16	SERVO AMPLIFIER INPUT (SENSOR)

Fig. 15 C


SERVO AMPLIFIER
NOR GATE
VCC SENSING
ACTIVE FILTER
MASTER MEMORY
SLAVE MEMORY
GATE PULSE AMPLIFIER
POTENTIOMETER TRANSLATION CIRCUIT
+Vcc
Vcc
P
Q
IC
R

gram

f = the supply frequency.
e.g. for a 380V ±10%, 50HZ supply, 1kW load
MAX. V_T of triac = 1.2V (@ I_L)
MAX. I_L of triac = 50mA

$$\text{we get } R_L = \frac{380^2}{10^3} = 144.4\Omega$$

$$R_L \text{ MAX} = 144.4 + 5\% = 152\Omega$$

$$V_L = I_L \times R_L + V_T = 0.05 \times 152 + 1.2 = 8.8\text{V Max}$$

The trailing edge of the firing pulse (Tf) must occur not sooner than

$$\frac{V_L \times 10^6}{V_{RMS} \times \sqrt{2} \times 2\pi f}\ \mu\text{s after the zero crossing point.}$$

$$\text{Tf MIN.} = \frac{8.8 \times 10^6}{0.9 \times 380 \times \sqrt{2} \times 2 \times \pi \times 50}$$

$$= 57.91\ \mu\text{s} = 24 \times C_D$$

$$\therefore \quad C_D \text{ MIN.} = 57.91 = 2.41\text{ nF}$$

$$\therefore \quad C_D = 2.7\text{ nF} \pm 10\%$$

The same triac could of course be used to control a higher power load. The load resistance and hence required V_L would fall, but for convenience the value of C_D need not be altered. Similarly, if the above calculations are repeated for a 220V supply, it will be established that C_D must exceed 1.77 nF and a value of 2.7 nF is again suitable. It may be convenient to use the same triac and value of C_D for 220, 240 and 380V applications. However, C_D should be kept as low as possible if power dissipation in the dropper resistor is to be minimised.

MAINS DROPPING RESISTOR (R_D)

Table I indicates the value of resistor R_D as a function of mains supply voltage, facilities provided etc. It will be apparent that it is desirable when dealing with a 380V supply to reduce power dissipation in the dropper resistor by introducing a series diode.

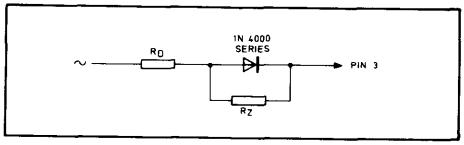


Fig. 14 Mains supply input circuit

	110V	220/ 240V	380V
R_Z ±10%	39k	82k	82k
Power dissipation in R_Z (max)	0.3W	0.4W	1W
Minimum value C_D	2.4 nF	1.9 nF	1.3 nF

Table 2 Max. value of R_Z for various supply voltages

The diode bypass resistor Rz (see Table 2) is necessary to provide proper operation of the zero voltage crossing circuit. The values for R_D given in the table may be reduced for rationalization purposes if required (e.g. common value for 220/240V supplies) or where additional external circuitry is fed by the 8.3V or 14V supplies. This may necessitate an appropriate increase in the value of the smoothing capacitor Cs. Furthermore, consideration should be given to the possible increase in chip power dissipation particularly if the external load is dynamic.

SMOOTHING CAPACITOR (Cs)

A 220µF 16V Capacitor should be used except when dealing with the higher current applications i.e. 5mA LED, 6mA buzzer etc. Cs should then be increased to 330µF. The ripple voltage should be kept below 1V peak – to – peak.

Facilities used					Nominal R_D value (±5%)	Maximum R_D power dissipation	Maximum R_D power dissipation (with diode)	Nominal power supply voltage ±10%	Nominal C_D
Room temperature control	Servo LED 0.5mA	Over temperature trip (security)	Servo LED 5mA	Security buzzer (6V, 6mA)					
●					3.3k	4.7W	2.3W	110V	4.7nF
●					7.5k	8.2W	4.1W	220V	
●					8.2k	8.9W	4.4W	240V	2.7nF
●					12k	15.3W	7.6W	380V	
●	●				3.0k	5.1W	2.5W	110V	4.7nF
●	●				6.8k	9.1W	4.5W	220V	
●	●				7.5k	9.8W	4.9W	240V	2.7nF
●	●				12k	15.3W	7.6W	380V	
●		●			3.0k	5.1W	2.5W	110V	4.7nF
●		●			6.8k	9.1W	4.5W	220V	
●		●			7.5k	9.8W	4.9W	240V	2.7nF
●		●			12k	15.3W	7.6W	380V	
●	●	●			3.0k	5.1W	2.5W	110V	4.7nF
●	●	●			6.8k	9.1W	4.5W	220V	
●	●	●			7.5k	9.8W	4.9W	240V	2.7nF
●	●	●			12k	15.3W	7.6W	380V	
●			●		2.2k	7.0W	3.5W	110V	4.7nF
●			●		5.1k	12.1W	6.0W	220V	
●			●		6.2k	11.8W	5.9W	240V	2.7nF
●			●		9.1k	20.2W	10.1W	380V	
●		●	●	●	2.2k	7.0W	3.5W	110V	4.7nF
●		●	●	●	4.7k	13.1W	6.5W	220V	
●		●	●	●	5.1k	14.4W	7.2W	240V	2.7nF
●		●	●	●	8.2k	22.4W	11.2W	380V	

Table 1 Value of R_D (mains dropping resistor)

PLESSEY
Semiconductors

SL446A

ZERO VOLTAGE SWITCH

Intended for use in ON/OFF control of triacs, the SL446A incorporates zero voltage point triggering in order to minimise radio frequency interference. Main application areas are in switching resistive loads and replacing mechanical thermostats in, for example, central heating systems, washing machine heaters, water heaters and smoothing irons.

The SL446A is suitable for mains on-line operation and requires minimal external components.

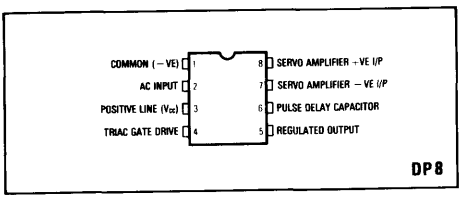


Fig. 1 Pin connections

FUNCTIONS

1. Balanced zero voltage point crossing detector, spike filter and pulse generator for reliable triggering of the triac.
2. A period pulse generator and bistable which are arranged to provide *symmetrical burst control* and *eliminate half-wave firing* (EN50,006/BS5406, 1976).
3. A high input impedance differential amplifier to form part of a servo system. An internally defined level of hysteresis is incorporated in the amplifier which can limit the rate of correction of the loop to meet the requirements of EN50,006/BS5406−1976, regarding flicker.
4. Internal rectification and regulation of current limited AC supply provides power for the IC and a suitable supply for the resistance bridge.
5. A supply voltage sensing circuit which inhibits firing pulses when the supply is inadequate to guarantee proper circuit operation. This effectively prevents firing pulses from being applied to the triac which are incapable of causing complete bulk conduction (possible failure mechanism at switch-on).

APPLICATIONS

- Pan Temperature Control
- Water Heaters
- Refrigerators
- Panel Heaters

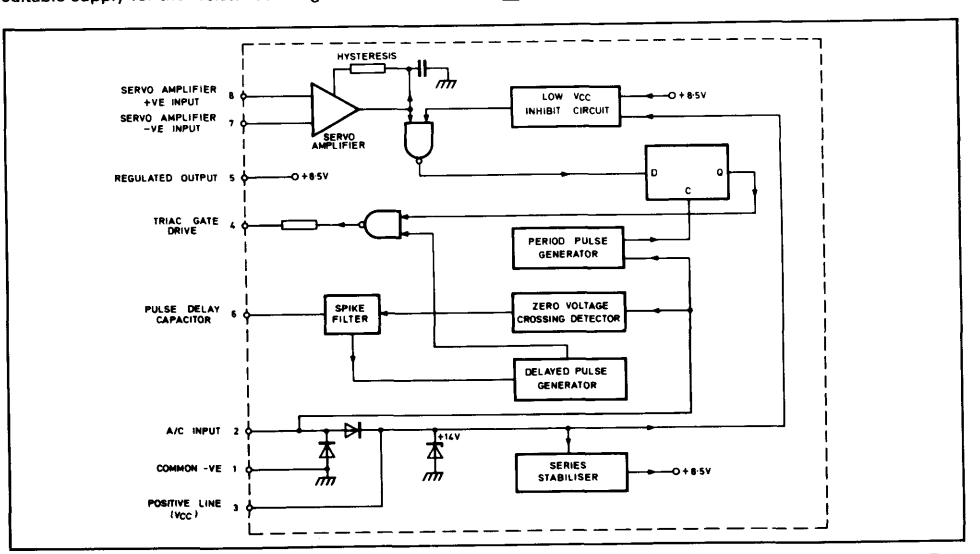


Fig. 2 SL446A block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)
$T_{AMB} = 25°C$,
All voltages measured with respect to common (pin 1)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Shunt regulating voltage pin 3		14.7		V	$I_3 = 16mA$
Shunt regulating voltage pin 3			16	V	$I_3 = 16mA$, $T_{amb} = +75°C$
Supply voltage trip level pin 3		12.2		V	
*Supply current (less I_4 AV, I_5)			7	mA	
Regulated voltage pin 5	8.0	8.5	9.0	V	
Regulated voltage temperature coefficient pin 5	−1		+1	mV/°C	
Triac gate drive pin 4					
Open circuit ON voltage		8.5		V	
Open circuit OFF voltage			0.1	V	
Output current into 2V drain	80	100		mA	
Output current into 4V drain	50	70		mA	
Output current into short circuit			200	mA	
Internal drain resistance		800		Ω	
Servo Amplifier input bias current			2	μA	
Servo Amplifier hysteresis	20	25	35	mV	
Servo Amplifier input offset voltage	−15	0	+15	mV	
Servo Amplifier input working voltage range	0		10	V	
Pin 6 output impedance R6	21.5	27	32.5	kΩ	
Maximum ripple voltage on supply pin 3			1	Vp-p	

★ The supply current is 0.45 x (RMS current fed into Pin 2)

Triac Firing Pulse

t_p Pulse width $= 0.69\ R6\ C_D$ μs typical
t_f Pulse finish $= 1.09\ R6\ C_D$ μs minimum after zero voltage point. (R6 in kΩ C_D in nF – See Fig.6.)
t_p Nominal ($C_D = 2.7nF$) $= 50\mu s$
t_f Minimum ($C_D = 2.7nF$) $= 63\mu s$

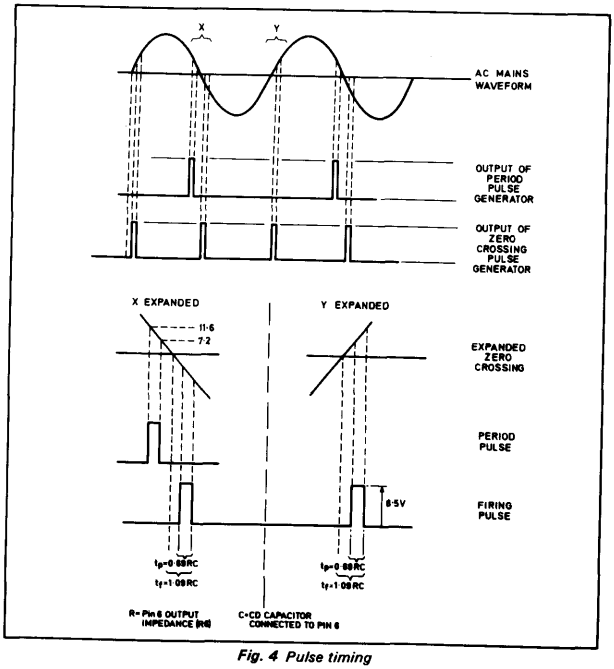


Fig. 4 Pulse timing

CIRCUIT DESCRIPTION

The externally current limited AC supply is applied to the device, and rectification followed by shunt regulation provides a 14V DC supply. This is externally smoothed before application to the 8.5V series stabiliser which feeds the resistance bridge. The stabiliser must be within regulation, or operation of the 'Low Vcc Inhibit' circuit will result. This circuit overrides all other circuitry and prevents unsuitable firing pulses from being supplied to the triac at 'switch-on'. The current limited AC supply also drives the Period Pulse Generator (PPG) and zero voltage crossing circuits.

The PPG produces a single short duration pulse for each completed mains cycle. The pulse train is used to clock logic information such that the circuit behaves in a symmetrical manner and only complete mains cycles are applied to the load.

The zero voltage crossing detector controls a pulse generator that has a delayed output. The delay is necessary since, with loads that are slightly inductive or low power resistive, the triac load current may not reach its required holding level at zero voltage point.

Both delay and pulse duration are defined by an external capacitor and this further serves the purpose of filtering out spikes which occur in the zero crossing region. Automatic rejection takes place of spikes having a duration of up to 50 per cent of the normal width of the triac firing pulse.

The servo amplifier has differential inputs and these are used to sense the output of the bridge. An internally defined level of hysteresis is incorporated in the amplifier; this can limit the rate of correction of the servo loop in order to meet the requirements of EN50,006/BS5406–1976. The output of the amplifier controls the logic circuitry and the triac is triggered on at the appropriate point in the mains cycle if pin 8 is more positive than pin 7.

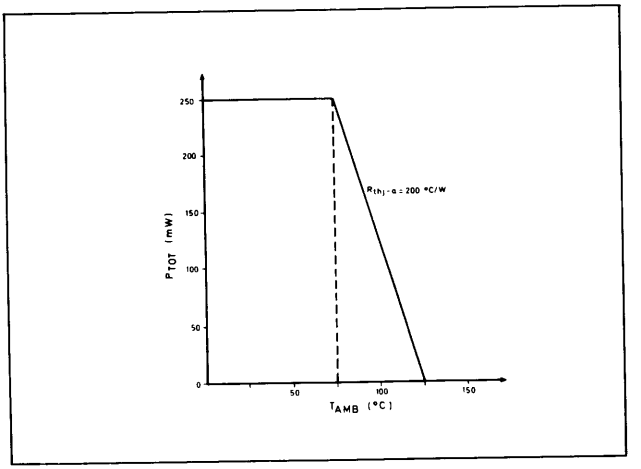
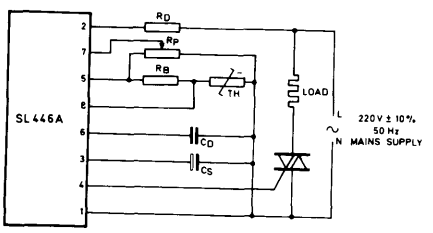


Fig. 3 Power dissipation

ABSOLUTE MAXIMUM RATINGS

Voltages		
Voltage on pins 7, 8	V_{7-1} ; V_{8-1}	V_3 (14V)
Voltage on pin 4	V_{4-1}	10V
Currents		
Supply current (pin 2) :		
Peak value $\pm I_{2M}$		50mA
Non-repetitive peak current (t_P<250µs) $\pm I_{2SM}$		200mA
Output current (pin 5)	I_5	10mA
Output current (pin 4), average value I_4 (AV)		10mA
Temperatures		
Operating ambient temperature	T_{AMB}	—10 to 75°C
Storage temperature	T_{STG}	—55 to ±125°C
Power Dissipation	See Fig. 3	

DESIGN EXAMPLE
(See application circuit Fig.5)



Components are to be standardised so that heating elements in the range 400 to 1200W may be used. The circuit is to provide linear temperature control over the domestic temperature range of +5°C to +35°C.

Fig. 5 Space heater application of the SL446A

Triac selection

The minimum load resistance is $\frac{V^2_{RMS}}{P} = \frac{220^2}{1200} =$ 40.33Ω.

Assuming a manufacturing tolerance of ±5% in the load resistance, the maximum load current is

$$\frac{220 \times 1.1}{40.33 \times 0.95} = 6.32\text{A RMS}$$

The peak repetitive mains voltage is $220 \times 2 \times 1.1 =$ 342V Max.

A suitable triac is the TAG 245–400. This is an isolated triac with ratings of 400V and 6.5A RMS at a case temperature of +70°C. The device is suitable for positive gate pulse operation and requires an I_{GT} of 50mA at a V_{GT} of 2.5V for reliable triggering. These triggering requirements are easily met since the SL446A delivers more than 50mA into a 4V drain. The trigger pulse width should be ⩾ 20 µs (see below).

Capacitor C_D

This capacitor defines both the delay and width of the triac firing pulse. The triac can not latch until the mains voltage exceeds the sum of the triac on-state voltage V_T and V_H which is the voltage dropped across the load resistance by the triac holding current I_H. ($V_T = 2.0$, $I_H = 50$mA for the TAG 245). The maximum load resistance corresponds to the 400W element.

$$\frac{V^2}{P} = \frac{220^2}{400} = 121\Omega$$

Maximum load resistance $= 121 \times 1.05 = 127\Omega$
$V_H + V_T = 6.35 + 2 = 8.35\text{V} = V_L$, i.e., triac latching can occur at the 8.35V point in the supply cycle.

It is necessary, therefore, to ensure that the firing pulse does not finish before this point in the supply cycle.

$$\text{Using } t_f \geqslant \frac{V_L}{V_M \times \sqrt{2} \times 2\pi f}$$

(V_M is the minimum RMS mains voltage, f is the supply frequency.)

$$t_f = \frac{8.35}{220 \times 0.9 \times \sqrt{2} \times 2 \times \pi \times 50}$$

$$t_f = 95\,\mu\text{s}$$

Using t_f Min. $= 1.09 \times C_D \times$ R6 Min. (R6 Min = 21.5kΩ)

$$C_D \quad \frac{95}{1.09 \times 21.5}\ \text{nF}$$

$$C_D \geqslant 4.05\text{nF}$$

Specify $C_D = 4.7\text{nF} \pm 10\%$ (Preferred value)

Using an ITT type KΩ223Y thermistor in a bridge comprising $R_B = 18\text{k}\Omega \pm 2\%$ and $R_p = 22\text{k}\Omega \pm 20\%$ linear potentiometer, substantially linear temperature control is obtained over the domestic temperature range +5°C to +35°C. The output from the bridge is approximately 100mV/°C and since the SL446A has a hysteresis of 25mV in the servo amplifier, the hysteresis of the thermostat is typically 0.25°C. The maximum bridge supply current occurs when V_5 equals 9.0V; the thermistor is at the maximum temperature and the potentiometer resistance is at minimum.

The characteristics of the thermistor are:

R_{25} = 22K ±10%
ß = 4300 ±5%

Using $R_{T1} = R_{T2} \times e^{\left(\frac{ß}{T_1} - \frac{ß}{T_2}\right)}$ and inserting R_{25} = −10% and ß = + 5% it is found that the resistance of the thermistor at 35°C (308°K) is 12.1k minimum.

$$I_5 = \frac{9}{22 \times 0.8} + \frac{9}{18 \times 0.98 \pm 12.1}\ \text{mA} =$$

0.814mA Max.

Average gate drive current I_4 (AV)

The maximum drive current is 200mA into a short circuit and this occurs for a period $2 \times t_p$ every mains cycle. It is acceptable to use the nominal value of R6 in the formula:

I_4 (AV) $= 2 \times t_p \times f \times 200$ mA and $t_p = 0.69\ C_D R6$
$= 2 \times (0.69 \times 4.7 \times 10^{-9} \times 27 \times 10^3)\ 50 \times 200$ mA
$= 1.75$mA

If C_D has a +10% tolerance.
I_4 (AV) $= 1.75 \times 1.1 = 1.925$mA Max.

Mains dropping resistor R_D

The total supply current of the circuit is $7.0\text{mA} + I_5 + I_4$ (AV) $= 7 + 0.814 + 1.925 = 9.74$mA Max.

$$\text{Using } R_D = \frac{\text{peak mains voltage} - V_3 \text{ Max.}}{\pi \times I_{3AV}}$$

$$R_D = \frac{220.0.9 \times \sqrt{2} - 16}{\pi \times 9.74}\ \text{k}\Omega \text{ Max.}$$

$R_D = 8.63$ kΩ Max.
Specify $R_D = 8.2$ kΩ ±5% (Preferred Value)

$$\text{The power dissipated by } R_D \text{ is} < \frac{V^2_{RMS} \text{ Max.}}{R_D \text{ Min.}}$$

$$< \frac{(220 \times 1.1)^2}{8.2 \times 0.95 \times 10^3}$$

Maximum power dissipated by R_D is 7.5 W.

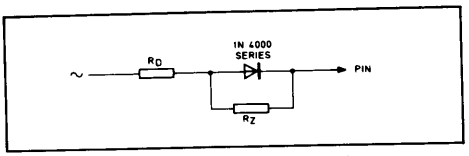


Fig. 6 Mains supply input circuit

The power dissipated by R_D is approximately halved if a series diode is used. However, the diode must be shunted with a bypass resistor for proper operation of the zero voltage crossing detector circuit. Suggested values for the by-pass resistor are 39kΩ for 110, 220 and 240V applications and 82kΩ for 380V operation. The diode should be rated to withstand the peak mains voltage. In the design example, the peak mains voltage is 220 × 1.1 × 2 = 342V and a 400V device is suggested.

Supply smoothing capacitor C_S

$$\text{Using } C \geqslant \frac{1}{f} \times \frac{3}{4} \times I_{3AV} = \frac{3 \times 9.74 \times 10^3}{50 \times 4}\ \mu F$$

$$C \geqslant 146\ \mu F.$$

Specify 220 μF −25%, +100%.

OPERATING NOTES

If any of the bridge components are distant from the IC additional spike filtering may be found necessary. An effective method is given below:

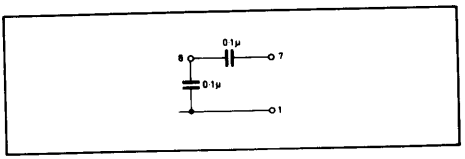
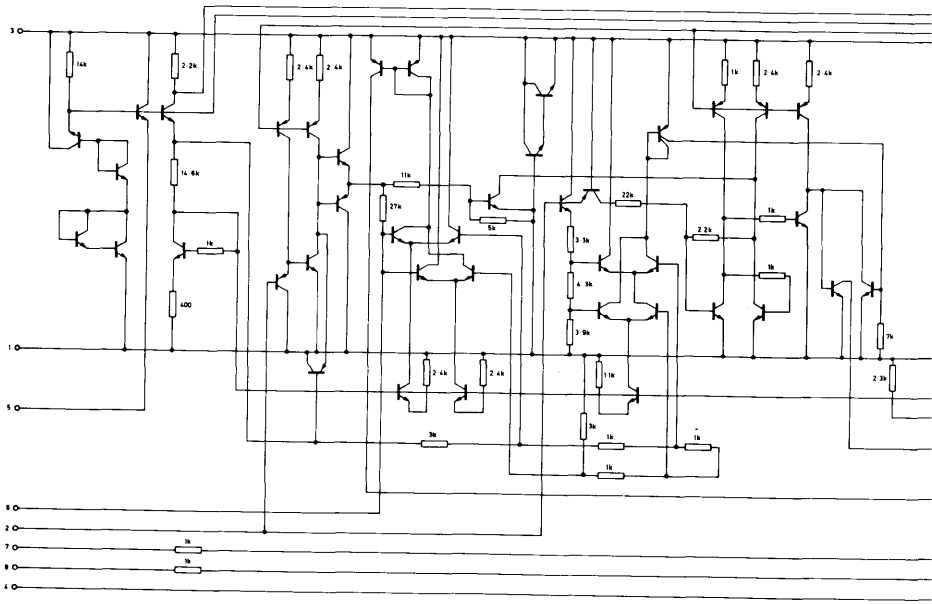


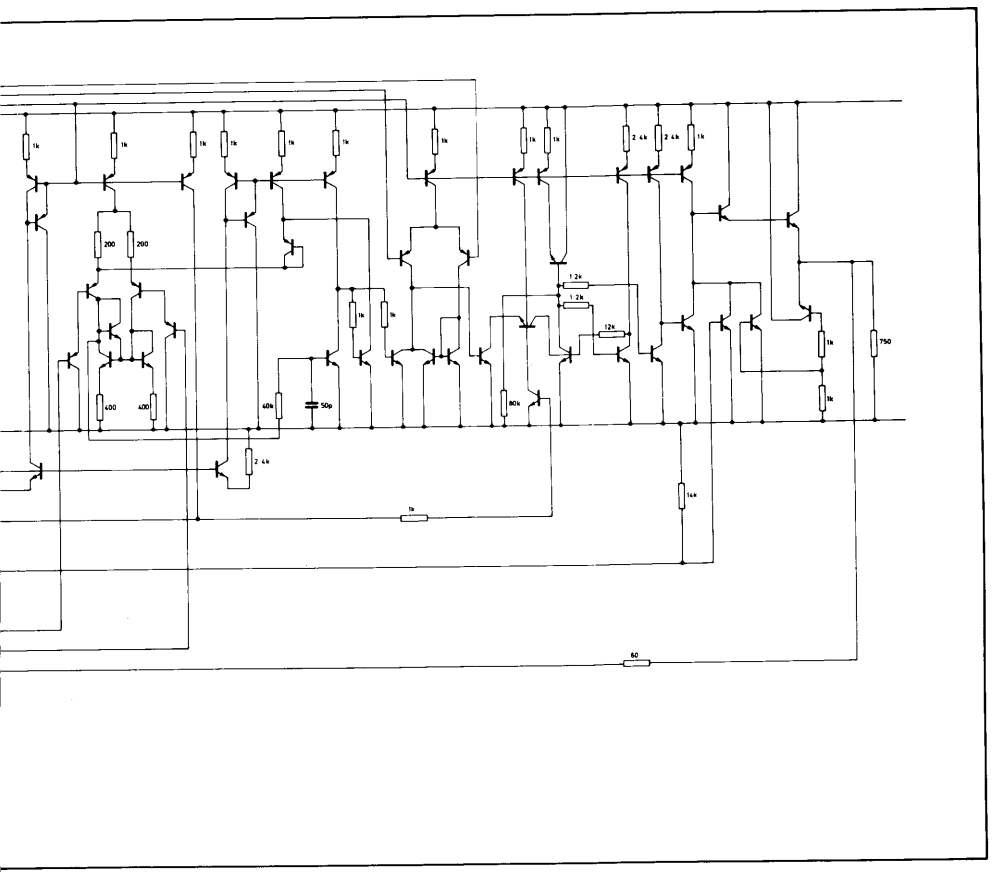
Fig. 7

If the mains dropping resistor is mounted on the main printed circuit board, board capacitance can couple spikes directly to the circuitry. It is good practice, therefore, to place a guard ring around the circuitry and take this to the common line (neutral, pin 1).



PIN	FUNCTION
1	COMMON (- VE)
2	A C INPUT
3	POSITIVE LINE
4	TRIAC GATE DRIVE
5	REGULATED OUTPUT
6	PULSE DELAY CAPACITOR
7	SERVO AMP -VE INPUT
8	SERVO AMP + VE INPUT

Fig. 8 C



ram

PLESSEY
Semiconductors

SL521A, B & C

WIDEBAND LOG AMPLIFIER

The SL521A, B and C are bipolar monolithic integrated circuit wideband amplifiers, intended primarily for use in successive detection logarithmic IF strips, operating at centre frequencies between 10MHz and 100MHz. The devices provide amplification, limiting and rectification, are suitable for direct coupling and incorporate supply line decoupling. The mid-band voltage gain of the SL521 is typically 12 dB (4 times). The SL521A, B and C differ mainly in the tolerance of voltage gain and upper cut-off frequency.

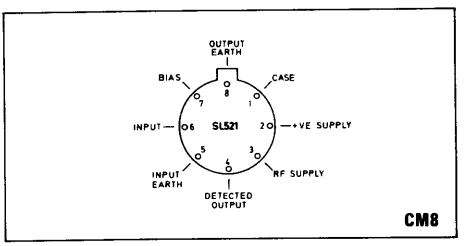


Fig. 1 Pin connections

FEATURES

- Well-defined Gain
- 4dB Noise Figure
- High I/P Impedance
- Low O/P Impedance
- 165MHz Bandwidth
- On-Chip Supply Decoupling
- Low External Component Count

APPLICATIONS

- Logarithmic IF strips with Gains up to 108 dB and Linearity Better Than 1 dB.

ABSOLUTE MAXIMUM RATINGS (Non-simultaneous)

Storage temperature range	−55°C to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance	250°C/W
Chip-to-case thermal resistance	80°C/W
Maximum instantaneous voltage at video output	+12V
Supply voltage	+9V

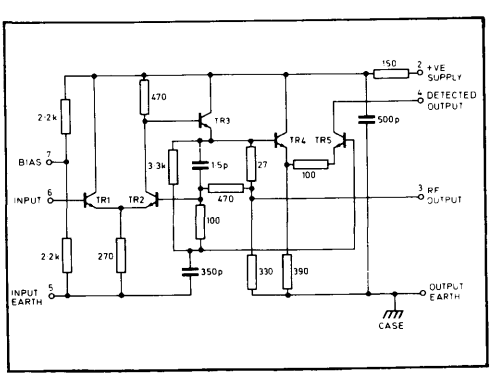


Fig. 2 SL521 Circuit diagram

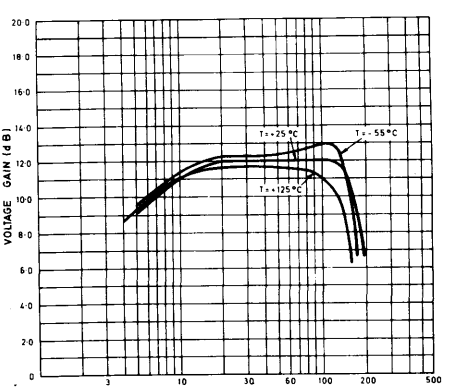


Fig. 3 Voltage gain v. frequency

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Temperature = +22°C ± 2°C
Supply voltage = +6V
DC connection between input and bias pins.

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Voltage gain, f = 30MHz	A	11.5		12.5	dB	
	B	11.3		12.7	dB	
	C	11.0		13.0	dB	10 ohms source, 8pF load
Voltage gain, f = 60MHz	A	11.3		12.7	dB	
	B	11.0		13.0	dB	
	C	10.7		13.3	dB	
Upper cut-off frequency (Fig. 3)	A	150	170		MHz	
	B	140	170		MHz	10 ohms source, 8pF load
	C	130	170		MHz	
Lower cut-off frequency (Fig. 3)	A B C		5	7	MHz	10 ohms source, 8pF load
Propagation delay	A B C		2		ns	
Maximum rectified video output current (Fig. 4 and 5)	A	1.00		1.10	mA	
	B	0.95		1.15	mA	f = 60MHz, 0.5V rms input
	C	0.90		1.20	mA	
Variation of gain with supply voltage	A B C		0.7		db/V	
Variation of maximum rectified output current with supply voltage	A B C		25		%/V	
Maximum input signal before overload	A B C	1.8	1.9		V rms	See note below
Noise figure (Fig. 6)			4	5.25	dB	f = 60MHz, Rs = 450 ohms
Supply current	A	12.5	15.0	18.0	mA	
	B	12.5	15.0	18.0	mA	
	C	11.5	15.0	19.0	mA	
Maxiumum RF output voltage			1.2		Vp-p	

Note: Overload occurs when the input signal reaches a level sufficient to forward bias the base-collector junction to TR1 on peaks.

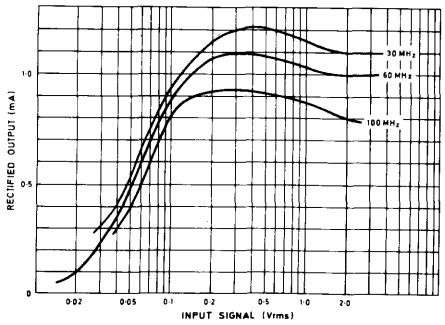


Fig. 4 Rectified output current v. input signal

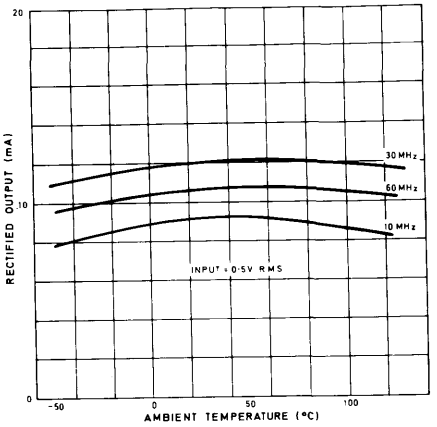


Fig. 5 Maximum rectified output current v. temperature

The 500pF supply decoupling capacitor has a resistance of, typically, 10 ohms. It is a junction type having a low breakdown voltage and consequently the positive supply current will increase rapidly if the supply voltage exceeds 7.5V (see ABSOLUTE MAXIMUM RATINGS).

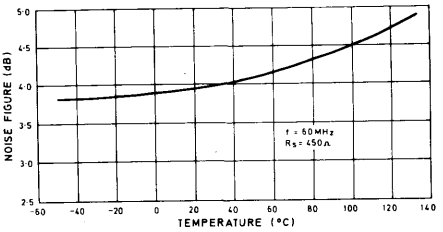


Fig. 6 Typical noise figure v. temperature

OPERATING NOTES

The amplifiers are intended for use directly coupled, as shown in Fig. 8.

The seventh stage in an untuned cascade will be giving virtually full output on noise.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The choice of network is also controlled by the need to avoid distorting the logarithmic law; the network must give unity voltage transfer at resonance. A suitable network is shown in Fig. 9. The value of C1 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit. Resistor R1 may be introduced to improve the symmetry of filter response, providing other values are adjusted for unity gain at resonance.

A simple capacitor may not be suitable for decoupling the output line if many stages and fast rises times are required. Alternative arrangements may be derived, based on the parasitic parameters given.

Values of positive supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in high frequency tuned cascades.

	Number of stages			
	6 or more	5	4	3
Minimum capacitance	30nF	10nF	3nF	1nF

The amplifiers have been provided with two earth leads to avoid the introduction of common earth lead inductance between input and output circuits. The equipment designer should take care to avoid the subsequent introduction of such inductance.

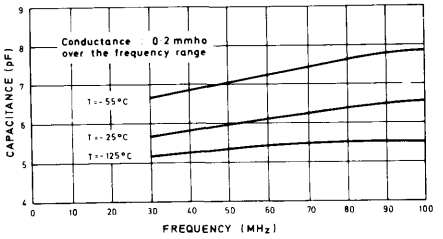


Fig. 7 Input admittance with open-circuit output

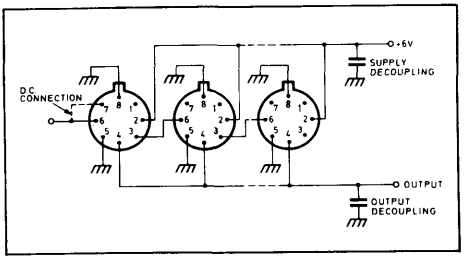


Fig. 8 Direct coupled amplifiers

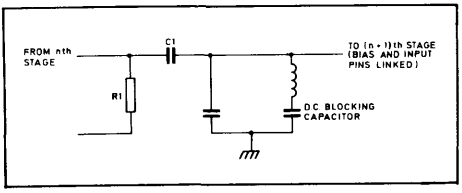


Fig. 9 Suitable interstage tuned circuit

Parasitic Feedback Parameters (Approximate)

The quotation of these parameters does not indicate that elaborate decoupling arrangements are required; the amplifier has been designed specifically to avoid this requirement. The parameters have been given so that the necessity or otherwise of further decoupling, may become a matter of calculation rather than guess-work.

$$\frac{\tilde{I}_4}{V_6} = \frac{\text{RF current component from pin 4}}{\text{Voltage at pin 6}} = 20 \text{ mmhos}$$

(This figure allows for detector being forward biased by noise signals)

$$\frac{V_6}{V_4} = \frac{\text{Effective voltage induced at pin 6}}{\text{Voltage at pin 4}} = 0.003$$

$$\frac{I_2}{V_6} = \frac{\text{Current from pin 2}}{\text{Voltage at pin 6}} = 6\text{mmhos (f = 10MHz)}$$

$$\left[\frac{V_6}{V_2}\right]_a = \frac{\text{Voltage induced at pin 6}}{\text{Voltage at pin 2}} = 0.03 \text{ (f = 10MHz)}$$

Voltage at pin 2
(pin 6 joined to pin 7 and fed from 300 ohms source)

$$\left[\frac{V_6}{V_2}\right]_b = \frac{\text{Voltage induced at pin 6}}{\text{Voltage at pin 2}} = 0.01 \text{ (f = 10MHz)}$$

Voltage at pin 2
(pin 7 decoupled)

$\frac{I_2}{V_6}\left[\frac{V_6}{V_2}\right]_a\left[\frac{V_6}{V_2}\right]_b$ decrease with frequency above 10MHz at 6 dB/octave.

PLESSEY
Semiconductors

SL523 B,C&H

DUAL WIDEBAND LOG AMPLIFIER

The SL523B and C are wideband amplifiers for use in successive detection logarithmic IF strips operating at centre frequencies between 10 and 100MHz. They are pin-compatible with the SL521 series of logarithmic amplifiers and comprise two amplifiers, internally connected in cascade. Small signal voltage gain is 24dB and an internal detector with an accurate logarithmic characteristic over a 20dB range produces a maximum output of 2.1mA. A strip of SL523s can be directly coupled and decoupling is provided on each amplifier. RF limiting occurs at an input voltage of 25mV RMS but the device will withstand input voltages up to 1.8V RMS without damage.

The SL523H is supplied in matched sets of eight devices. The gain at 60MHz of the devices in the set is matched to 0.75dB. In all other respects the device is identical to an SL523B. This selection enables very precise log strips to be produced.

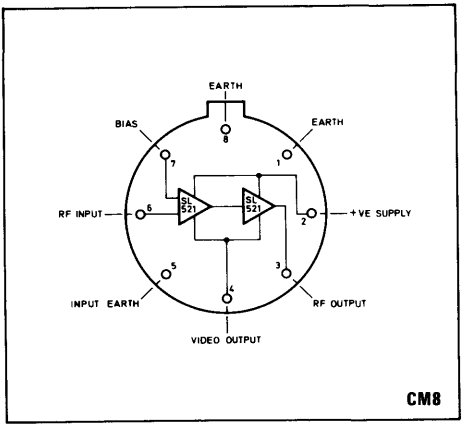


Fig. 1 Pin connections (view from beneath)

FEATURES

- Small Size/Weight
- Lower Power Consumption
- Readily Cascadable
- Accurate Logarithmic Detector Characteristic

QUICK REFERENCE DATA

Small Signal Voltage Gain	24dB
Detector Output Current	2.1mA
Noise Figure	4dB
Frequency Range	10 – 100MHz
Supply Voltage	+6V
Supply Current	30mA

ABSOLUTE MAXIMUM RATINGS

(Non simultaneous)

Storage temperature range —55°C to + 175°C
Operating temperature range —55°C to +125°C
Maximum instantaneous voltage at video output +12V
Supply voltage +9V

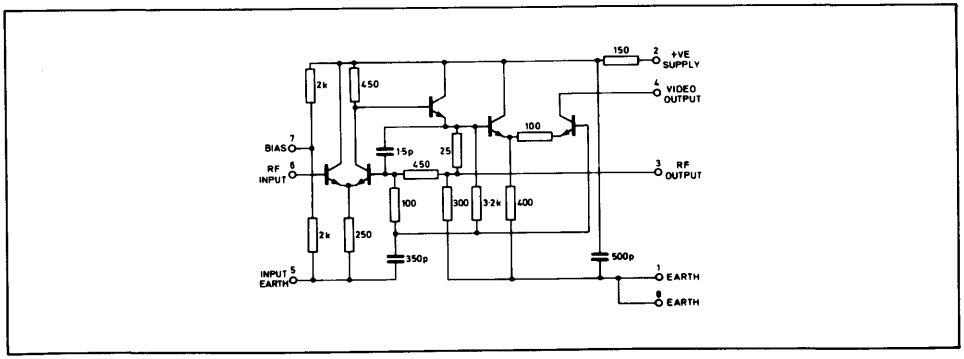


Fig. 2 Circuit diagram (one amplifier)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Ambient temperature 22°C ±2°C
Supply voltage +6V
DC connection between pins 6 and 7
Source impedance 10Ω
Load impedance 8pF
Frequency 60MHz

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Small signal voltage gain	B H	22.6	24	25.4	dB	Freq. 30MHz
	C	22	24	26	dB	
Small signal voltage gain	B H	22	24	26	dB	Freq. 60MHz
	C	21.4	24	26.6	dB	
Gain variation (set of 8)	H		0.5	0.75	dB	Freq. = 60MHz
Upper cut off frequency	B C & H	120	150		MHz	
Lower cut-off frequency	B C & H		10	15	MHz	
Propagation delay	B C & H		4		ns	
Maximum rectified video output current	B H	1.9	2.1	2.3	mA	V_{in} 0.5VRMS
	C	1.8	2.1	2.4	mA	
Maximum input signal before overload	B C & H	1.8	1.9		VRMS	
Noise figure			4	5.25	dB	Source impedance 450Ω
Supply current	B H	25	30	36	mA	
	C	23	30	38	mA	
Maximum RF output voltage	B C & H		1.2		Vp-p	

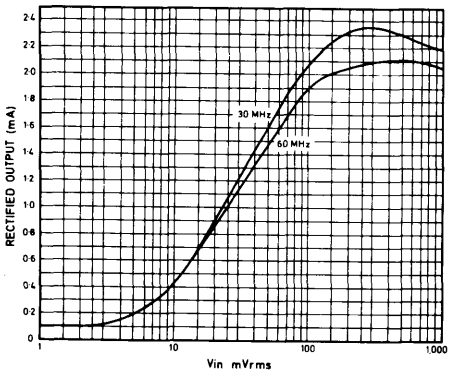


Fig. 3 Rectified output current v. input signal

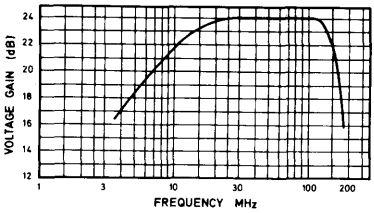


Fig. 4 Voltage gain v. frequency

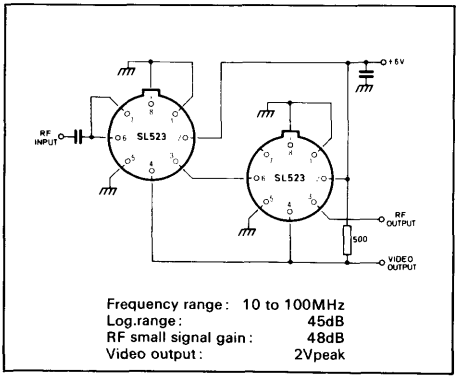


Fig. 5 Simple log.IF strip

OPERATING NOTES

The amplifier is designed to be directly coupled (see Fig. 5)

The fourth stage in an untuned cascade will give full output on the broad band noise generated by the first stage.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The network chosen must give unity voltage gain at resonance to avoid distorting the log law. The typical value for input impedance is 500 ohms in parallel with 5pF and the output impedance is typically 30 ohms.

Although a 1nF supply line decoupling capacitor is included in the can an extra capacitor is required when the amplifiers are cascaded. Minimum values for this capacitor are: 2 stages – 3nF, 3 or more stages – 30nF.

In cascades of 3 or more stages care must be taken to avoid oscillations caused either by inductance common to the input and output earths of the strip or by feedback along the common video line. The use of a continuous earth plane will avoid earth inductance problems and a common base amplifier in the video line isolating the first two stages as shown in Fig.6 will eliminate feedback on the video line.

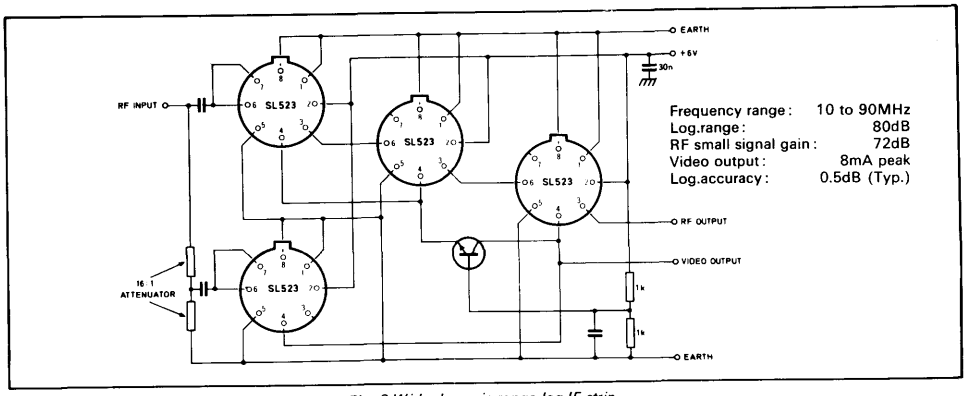


Fig. 6 Wide dynamic range log.IF strip

TYPICAL PERFORMANCE

Unselected SL523B devices were tested in a wide-band logarithmic amplifier, described in RSRE Memo. No.3027 and shown in Fig. 7.
The amplifier consists of six logarithmic stages and two 'lift' stages, giving an overall dynamic range of greater than 80dB. The response and error curves were plotted on an RHG Log Test Set and bandwidth measurements were made with a Telonic Sweeper and Tektronix oscilloscope.

Fig. 8 shows the dynamic range error curve and frequency response obtained. The stage gains of the SL523 devices used were as shown in Table 1.

Stages	f_o (MHz)	Gain (dB)	Max. Deviation (dB)
1	60	24.123	
2	60	24.089	0.235
3	60	23.888	
Lift	60	24.086	

Table 1 Stage gains of SL523 used in performance tests

The input v. output characteristic (Fig. 8a) is calibrated at 10dB/cm in the X axis and 1V/cm in the Y axis. 80dB of dynamic range was attained.

The error characteristic (Fig. 8b) is calibrated at 10dB/cm in the X axis and 1dB/cm in the Y axis; this shows the error between the log. input v. output characteristic and a mean straight line and shows that a dynamic range of 80dB was obtained with an accuracy of $\pm$0.5dB.

As a comparison, the log amplifier of Fig. 7 was constructed with randomly selected SL521Bs (two SL521Bs replacing each SL523B). Again, a dynamic response of 80dB was obtained (Fig. 9a) with an accuracy of $\pm$0.75dB (Fig. 9b).

Bandwidth curves are shown in Figs. 8c and 9c, where the amplitude scale is 2dB/cm, with frequency markers at 10MHz intervals from 20 to 100MHz. Using SL523Bs (Fig. 8c), the frequency response at 90MHz is 4dB down on maximum and there is a fall-off in response after 50MHz. Fig. 9c shows that the frequency response of the amplifier falls off more gradually after 40MHz but again the response at 90MHz is 4dB down on maximum.

These tests show that the SL523 is a very successful dual-stage log.amplifier element and, since it is pin-compatible with the SL521, enables retrofit to be carried out in existing log.amplifiers. It will be of greatest benefit however, in the design of new log amplifiers, enabling very compact units to be realised with a much shorter summation line.

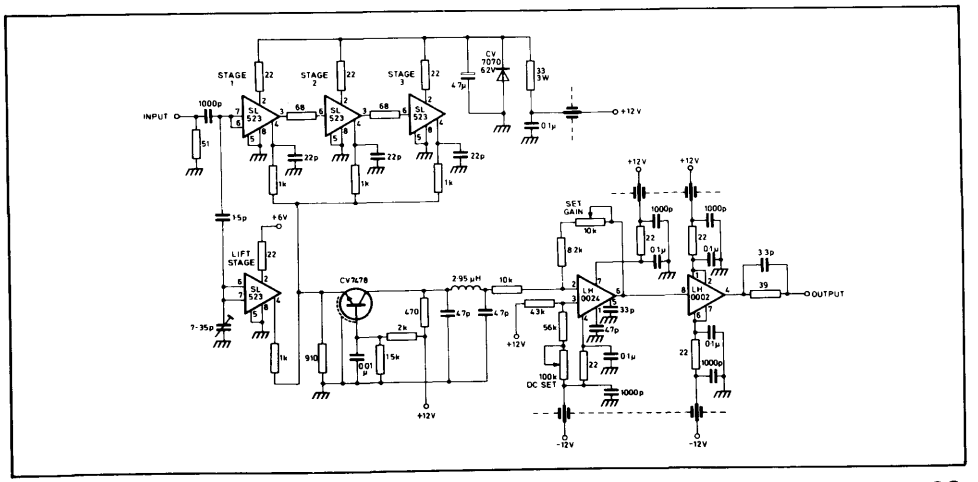


Fig. 7 Wideband logarithmic amplifier

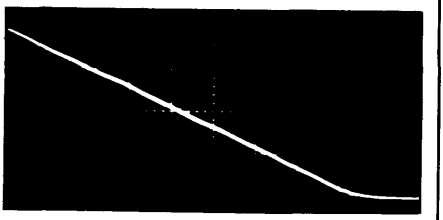


Fig. 8a Input/output

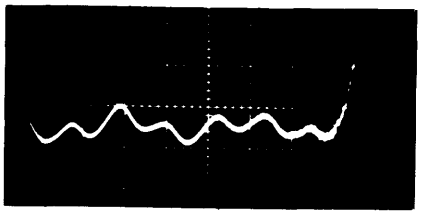


Fig. 8b Error curve

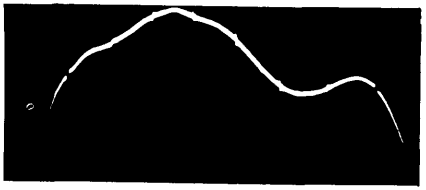


Fig. 8c Frequency response, detected output

Fig. 8 Characteristics of circuit shown in Fig. 7 using SL523Bs

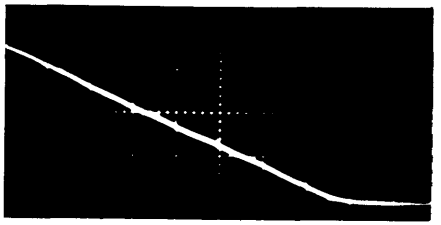


Fig.9a Input/output

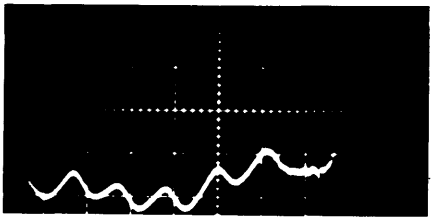


Fig. 9b Error curve

Fig. 9c Frequency response, detected output

Fig. 9 Characteristics of circuit shown in Fig. 7 using SL521Bs

PLESSEY
Semiconductors

SL525C

120MHz WIDEBAND LOG IF STRIP AMPLIFIER

The SL525C is a bipolar monolithic integrated circuit wideband amplifier, intended primarily for use in successive detection logarithmic I.F. strips, operating at centre frequencies between 10MHz and 60MHz. The devices provide amplification, limiting and rectification, are suitable for direct coupling and incorporate supply line decoupling. The mid-band voltage gain of the SL525C is typically 12dB.

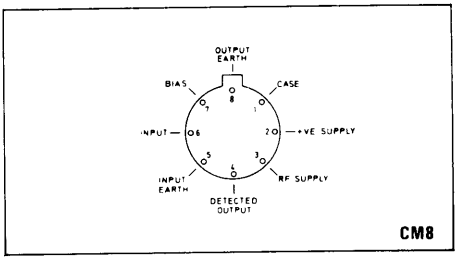


Fig.1 Pin connections

FEATURES

- Well-defined Gain
- 4dB Noise Figure
- High I/P Impedance
- Low O/P Impedance
- 150 MHz Bandwidth
- On-Chip Supply Decoupling
- Low External Component Count

APPLICATIONS

- Logarithmic IF strips with Gains up to 108 dB and Linearity Better Than 1 dB.

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	−55°C to +175°C
Operating Temperature range	−20°C to +100°C
Maximum instantaneous voltage at video output	+12V
Supply voltage	9V

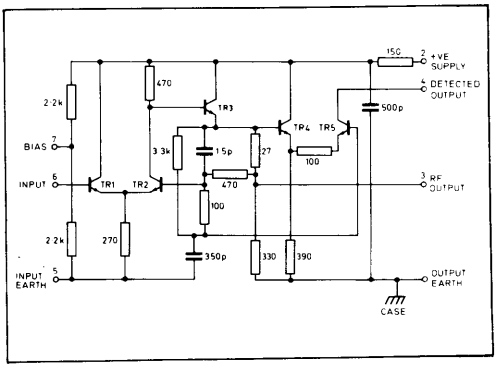


Fig.2 Circuit diagram

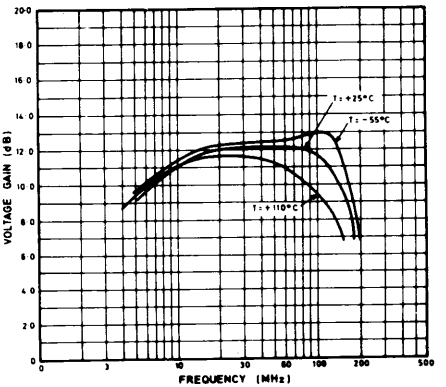


Fig.3 Voltage gain v. frequency

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):–
T_A = +22°C ±2°C
Supply voltage = +6V
DC connection between input and bias pins

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	10.5		13.5	dB	f = 30MHz, R_S = 10Ω, C_L = 8pF
	10.0		14.0	dB	f = 60MHz, R_S = 10Ω, C_L = 8pF
Upper cut-off frequency (Fig. 3)	120	150		MHz	R_S = 10Ω, C_L = 8pF
Lower cut-off frequency (Fig. 3)		5	7	MHz	R_S = 10Ω, C_L = 8pF
Propagation delay		2		ns	
Max. rectified video output current (Figs. 4 and 5)	0.85		1.25	mA	f = 60MHz, V_{in} = 500mV rms
Variation of gain with supply voltage		0.7		dB/V	
Variation of maximum rectified output current with supply voltage		25		%/V	
Maximum I/P signal before overload	1.8	1.9		Vrms	See note 1
Noise figure (Fig. 6)		4	5.25	dB	f = 60MHz, R_S = 450Ω
Maximum RF output voltage		1.2		Vp-p	
Supply current		15		mA	

NOTE

1. Overload occurs when the input signal reaches a level sufficient to forward-bias the base-collector junction of TR1 on peak.

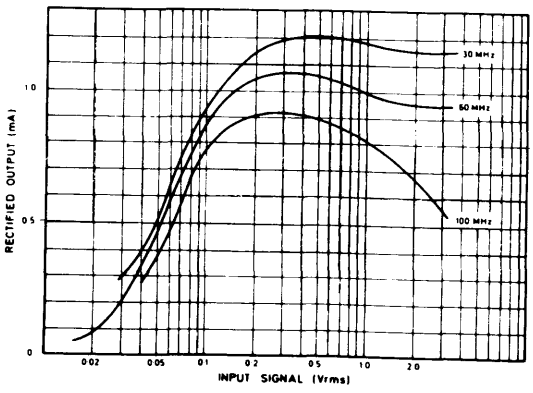


Fig. 5 Rectified output current v. input signal

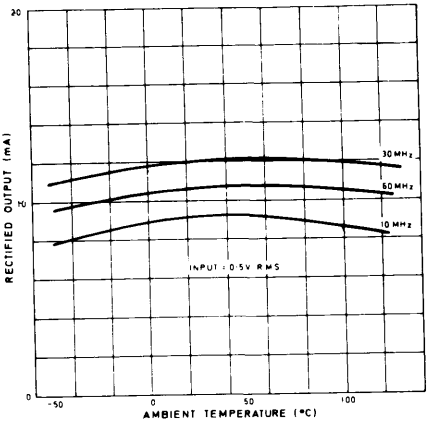


Fig. 5 Maximum rectified output current v. temperature

The 500pF supply decoupling capacitor has a resistance of, typically, 10 ohms. It is a junction type having a low breakdown voltage and consequently the positive supply current will increase rapidly if the supply voltage exceeds 7.5V (see ABSOLUTE MAXIMUM RATINGS).

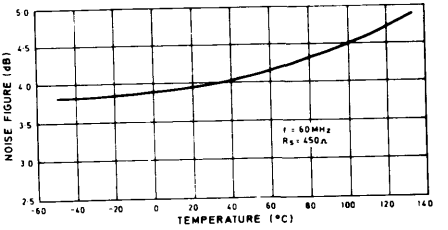


Fig. 6 Typical noise figure v. temperature

OPERATING NOTES

The amplifiers are intended for use directly-coupled, as shown in Fig. 8

The seventh stage in an untuned cascade will be giving virtually full output on noise.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The choice of network is also controlled by the need to avoid distorting the logarithmic law; the network must give unity voltage transfer at resonance. A suitable network is shown in Fig. 9. The value of C1 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit. Resistor R1 may be introduced to improve the symmetry of filter response, providing other values are adjusted for unity gain at resonance.

A simple capacitor may not be suitable for decoupling the output line if many stages and fast rises times are required.

Values of positive supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in high frequency tuned cascades.

	Number of stages			
	6 or more	5	4	3
Minimum capacitance	30nF	10nF	3nF	1nF

The amplifiers have been provided with two earth leads to avoid the introduction of common earth lead inductance between input and output circuits. The equipment designer should take care to avoid the subsequent introduction of such inductance.

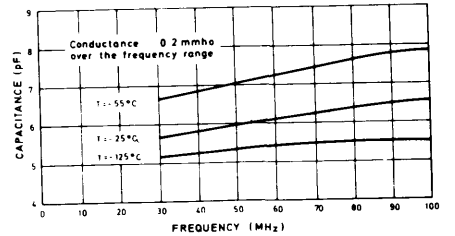


Fig. 7 Input admittance with open-circuit output

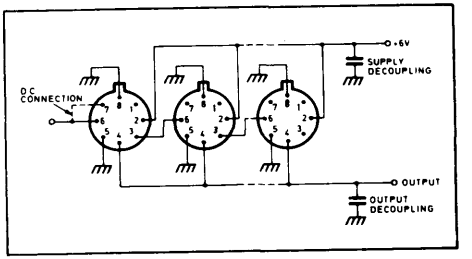


Fig. 8 Direct coupled amplifiers

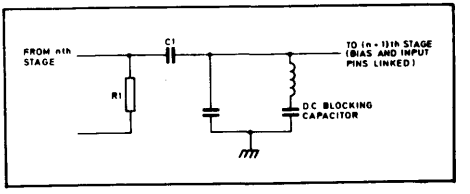


Fig. 9 Suitable interstage tuned circuit

Parasitic Feedback Parameters (Approximate)

The quotation of these parameters does not indicate that elaborate decoupling arrangements are required; the amplifier has been designed specifically to avoid this requirement. The parameters have been given so that the necessity or otherwise of further decoupling, may become a matter of calculation rather than guess-work.

$$\frac{\tilde{I}_4}{V_6} = \frac{\text{RF current component from pin 4}}{\text{Voltage at pin 6}} = 20 \text{ mmhos}$$

(This figure allows for detector being forward biased by noise signals)

$$\frac{V_6}{V_4} = \frac{\text{Effective voltage induced at pin 6}}{\text{Voltage at pin 4}} = 0.003$$

$$\frac{I_2}{V_6} = \frac{\text{Current from pin 2}}{\text{Voltage at pin 6}} = 6\text{mmhos (f = 10MHz)}$$

$$\left[\frac{V_6}{V_2}\right]_a = \frac{\text{Voltage induced at pin 6}}{\text{Voltage at pin 2}} = 0.03 \text{ (f = 10MHz)}$$

Voltage at pin 2
(pin 6 joined to pin 7 and
fed from 300 ohms source)

$$\left[\frac{V_6}{V_2}\right]_b = \frac{\text{Voltage induced at pin 6}}{\text{Voltage at pin 2}} = 0.01 \text{ (f = 10MHz)}$$

Voltage at pin 2
(pin 7 decoupled)

$\frac{I_2}{V_6}$ $\left[\frac{V_6}{V_2}\right]_a$ $\left[\frac{V_6}{V_2}\right]_b$ decrease with frequency above 10MHz at 6 dB/octave.

PLESSEY
Semiconductors

SL531C

TRUE LOG IF AMPLIFIER

The SL531C is a wide band amplifier designed for use in logarithmic IF amplifiers of the true log type. The input and log output of a true log amplifier are at the same frequency i.e. detection does not occur. In successive detection log amplifiers (using SL521, SL1521 types) the log output is detected.

The small signal gain is 10dB and bandwidth is over 500MHz. At high signal levels the gain of a single stage drops to unity. A cascade of such stages give a close approximation to a log characteristic at centre frequencies between 10 and 200MHz.

An important feature of the device is that the phase shift is nearly constant with signal level. Thus any phase information on the input signal is preserved through the strip.

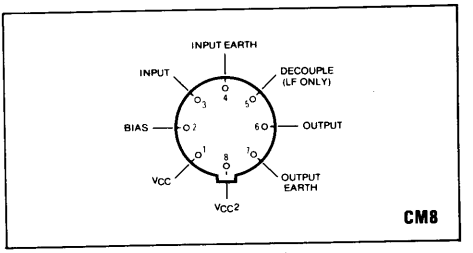


Fig. 1 Pin connections

FEATURES

- Low Phase Shift vs Amplitude
- On-Chip Supply Decoupling
- Low External Components Count

APPLICATIONS

True Log Strips with: –

- Log Range 70 dB
- Centre frequencies 10 – 200 MHz
- Phase Shift ± 0.5 degrees / 10 dB

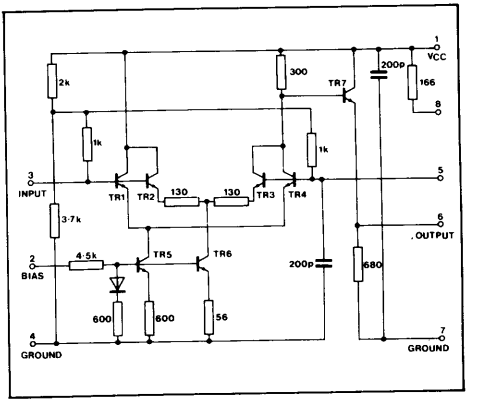


Fig. 2 Circuit diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+15 volts
Storage temperature range	−55°C to + 150°C
Operating temperature range	−55°C to +125°C
	See operating notes
Max junction temperature	150°C
Junction — ambient thermal resistance	220°C/Watt
Junction — case thermal resistance	80°C/Watt

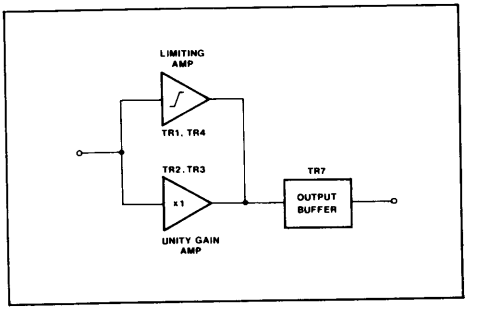


Fig. 3 Block diagram

CIRCUIT DESCRIPTION

The SL531 transfer characteristic has two regions. For small input signals it has a nominal gain of 10 dB, at large signals the gain falls to unity (see Fig 7). This is achieved by operating a limiting amplifier and a unity gain amplifier in parallel (see Fig 3). Tr1 and Tr4 comprise the long tailed pair limiting amplifier, the tail current being supplied by Tr5, see Fig 2. Tr2 and Tr3 form the unity gain amplifier the gain of which is defined by the emitter resistors. The outputs of both stages are summed in the 300 ohm resistor and Tr7 acts as an emitter follower output buffer. Important features are the amplitude and phase linearity of the unity gain stage which is achieved by the use of 5GHz transistors with carefully optimised geometries.

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Test circuit Fig (4)
Frequency 60 MHz
Supply voltage 9 volts
Ambient temperature 22± 2°C

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Small signal voltage gain	8	10	12	dB	Vin = −30 dBm
High level slope gain	−1	0	+1	dB	
Upper cut off frequency	250	500		MHz	
Lower cut off frequency		3	10	MHz	−3dB w.r.t. ± 60 MHz
Supply current		17	25	mA	
Phase change with input amplitude		1.1	3	degrees	Vin − 30 dBm to + 10 dBm
Input impedance	2.5pf parallel with 1k				10 − 200MHz
Output impedance	15Ω series with 25nh				

OPERATING NOTES

1. Supply Voltage Options

An on chip resistor is provided which can be used to drop the supply voltage instead of the external 180 ohms shown in the test circuit. The extra dissipation in this resistor reduces the maximum ambient operating temperature to 100°C. It is also possible to use a 6 volt supply connected directly to pins 1 and 2. Problems with feedback on the supply line etc may occur in this connection and RF chokes may be required in the supply line between stages.

2. Layout Precautions

The internal decoupling capacitors help prevent high frequency instability, however normal high frequency layout precautions are still necessary. Coupling capacitors should be physically small and be connected with short leads. It is most important that the ground connections are made with short leads to a continuous ground plane.

3. Low Frequency Response

The LF response is determined by the on chip capacitors. It can be extended by extra external decoupling on pins 5 and 1.

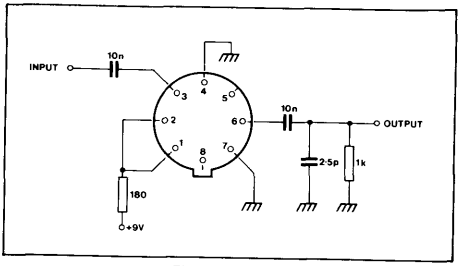


Fig. 4 Test circuit

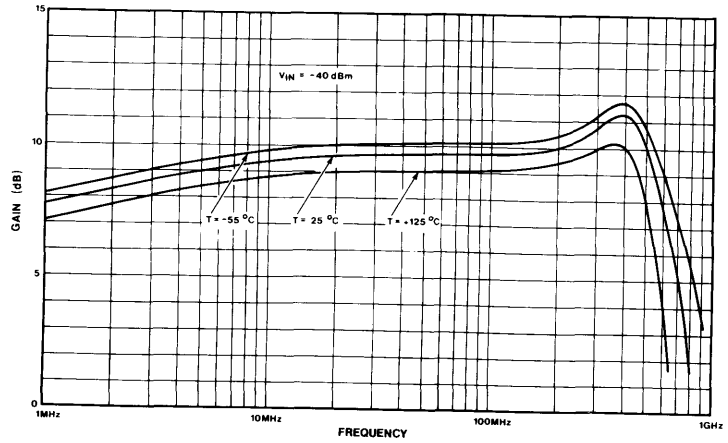


Fig. 5 Small signal frequency response

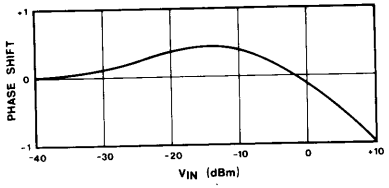


Fig. 6 Phase v. input

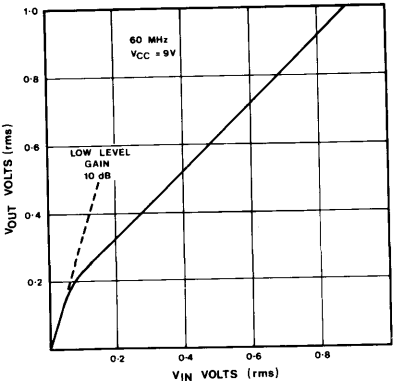


Fig. 7 Transfer characteristics linear plot

TYPICAL APPLICATION — 6 STAGE LOG STIP

Input log range 0dBm to −70dBm
Low level gain 60dB (−70dBm in)
Output dynamic range 20dB
Phase shift (over log range) ±3°
Frequency range 10 — 200MHz

The circuit shown in Fig 9 is designed to illustrate the use of the SL531 in a complete strip. The supply voltage is fed to each stage via an external 180Ω resistor to allow operation to 125°C ambient. If the ambient can be limited to + 100°C then the internal resistor can be used to reduce the external component count. Interstage coupling is very simple with just a capacitor to isolate bias levels being necessary. No connection is necessary to pin 5 unless operation below 10MHz is required. It is important to provide extra decoupling on pin 1 of the first stage to prevent positive feedback occuring down the supply line. An SL560 is used as a unity gain buffer, the output of the log strip being attenuated before the SL560 to give a nominal 0dBm output into 50Ω.

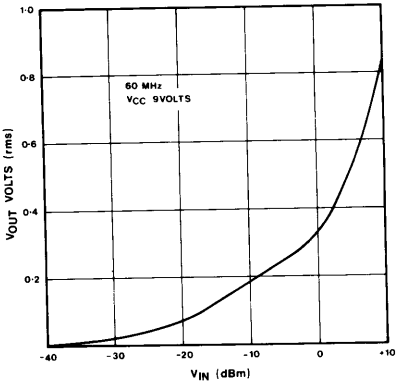


Fig. 8 Transfer characteristics logarithmic input scale

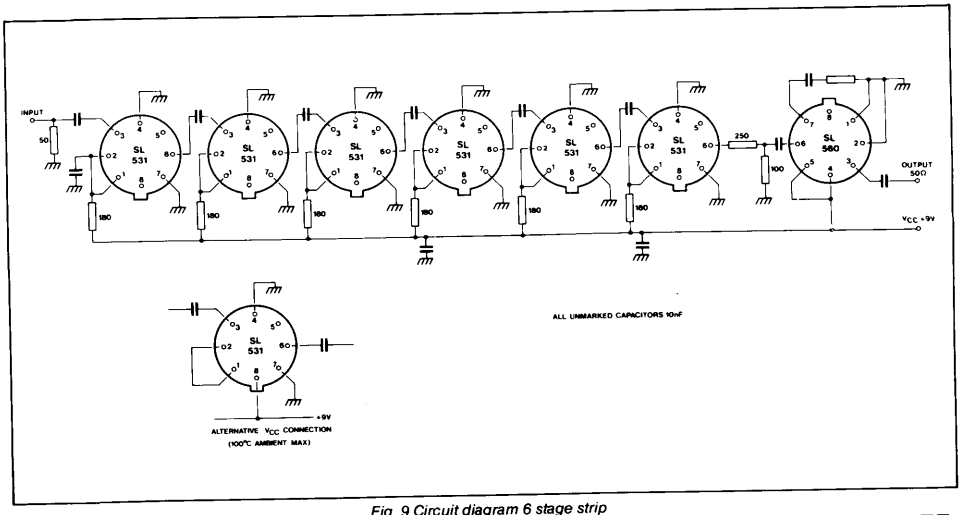


Fig. 9 Circuit diagram 6 stage strip

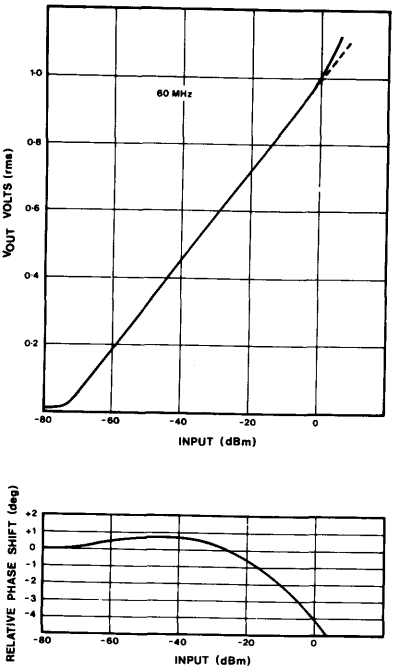


Fig. 10 Transfer function of log strip

PLESSEY
Semiconductors

SL532C

LOW PHASE SHIFT LIMITER

The SL532C is a monolithic integrated circuit designed for use in wide band limiting IF strips. It offers a bandwidth of over 400MHz and very low phase shift with amplitude. The small signal gain is 12dB and the limited output is 1volt peak to peak. The use of a 5GHz IC process has produced a circuit which gives less than 1° phase shift when overdriven by 12dB. The amplifier has internal decoupling capacitors to ease the construction of cascaded strips and the number of external components required has been minimised.

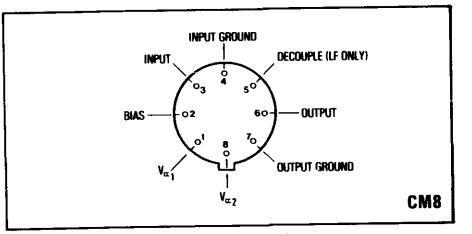


Fig.1 Pin connections

FEATURES

- Low Phase Shift v. Amplitude
- Wide Bandwidth
- Low External Component Count

APPLICATIONS

- Phase Recovery Strips in Radar and ECM Systems (e.g. Doppler)
- Limiting Amps for SAW Pulse Compression Systems
- Phase Monopulse Radars
- Phased Array Radars
- Low Noise Oscillators

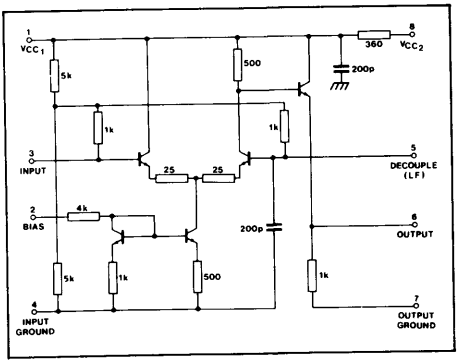


Fig.2 Circuit diagram

ELECTRICAL CHARACTERISTICS

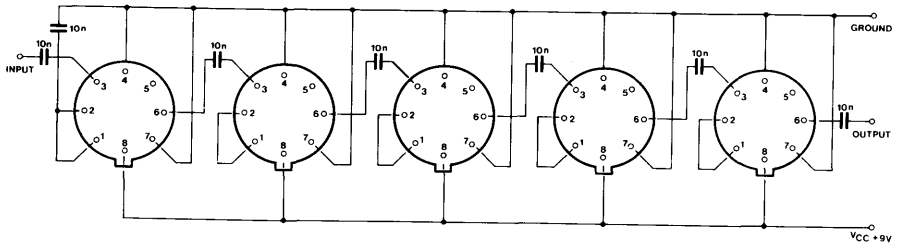
Test conditions (unless otherwise stated):
Temperature (Ambient) 25°C
Frequency 60MHz
V_{CC} = +9V
R_L = 1kΩ//2.5pF

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Small signal voltage gain	10	12	14	dB	
Limited output voltage	0.9	1.2	1.55	Vp-p	
Upper cut off frequency	200	400		MHz	-3dB. The lower frequency cut off can be extended by the use of external capacitors
Lower cut off frequency		7.5	10	MHz	
Supply current		8.5	11	mA	
Phase variation with signal level		±1		degree	V_{IN} = -30dBm to +10dBm
Input impedance		1kΩ//2.5pF			
Output impedance		30Ω			
Max input signal before overload		+20		dBm	
Gain variation with temperature		1		dB	55°C to +125°C
Noise figure		7		dB	400Ω source impedance at 60MHz

TYPICAL APPLICATION

Five stage strip

Input signal for full limiting	300μV rms −57dBm
Limited output	1V p-p
Phase shift (V_{IN} −57 → +10dBm)	±3° typ.



The recommended output buffer amplifier to drive 50Ω loads is the SL560C

Fig.3 Five stage IF strip

CIRCUIT DESCRIPTION

The SL532 uses a long-tailed pair limiting amplifier which combines low phase shift with a symmetrical limiting characteristic. This is followed by a simple emitter follower output stage. Each stage of a strip is capable of driving to full output a succeeding SL532 but a buffer amplifier is needed to drive lower impedance loads. No external decoupling capacitors are normally required but for use below 10MHz extra decoupling can be added on pins 1 and 5. Bias for the long-tailed pair is provided by connecting the bias (pin 2) to the decoupled supply (pin 1).

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+15V
Storage temperature range	−55°C to +150°C
Operating temperature range	−55°C to +125°C

PLESSEY
Semiconductors

SL541B

HIGH SLEW RATE OPERATIONAL AMPLIFIERS

The SL541 is a monolithic amplifier designed for optimum pulse response and applications requiring high slew rate with fast settling time to high accuracy. The high open loop gain is stable with temperature, allowing the desired closed loop gain to be achieved using standard operational amplifier techniques. The device has been designed for optimum response at a gain of 20dB when no compensation is required. The SL541B has a guaranteed input offset voltage of ±5mV maximum and replaces the SL541C.

The SL541B is tested in two circuit applications (A and B).

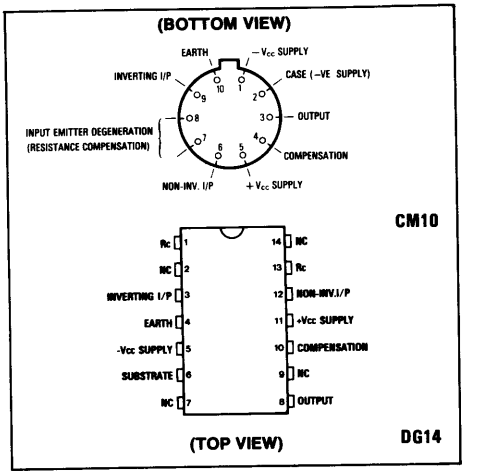


Fig. 1 Pin connections

FEATURES

- High Slew Rate: 175V/μs
- Fast Settling Time: 1% in 50ns
- Open Loop Gain: 70dB (SL541B)
- Wide Bandwidth: DC to 100MHz at 10dB Gain
- Very Low Thermal Drift: 0.02dB/°C Temperature Coefficient of Gain
- Guaranteed 5mV input offset maximum
- Full Military Temperature Range (DIL Only)

Package: 10 Lead TO-5
14 Lead DIL Ceramic

APPLICATIONS

- Wideband IF Amplification
- Wideband Video Amplification
- Fast Settling Pulse Amplifiers
- High Speed Integrators
- D/A and A/D Conversion
- Fast Multiplier Preamps

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V+ to V−)	24V
Input voltage (Inv. I/P to non inv. I/P)	±9V
Storage temperature	−55°C to +175°C
Chip operating temperature	+175°C
Operating temperature:	TO-5: −55°C to +85°C
	DIL: −55°C to +125°C

Thermal resistances

Chip-to-ambient:	TO-5	220°C/W
	DIL	125°C/W
Chip-to-case:	TO-5	60°C/W
	DIL	40°C/W

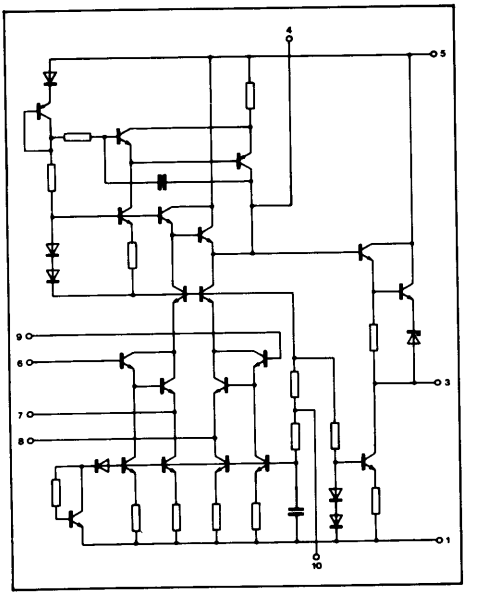


Fig. 2 SL541 circuit diagram (TO-5 pin nos.)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 25° C

R_C = 0Ω

Test circuits: see Fig.8

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Static nominal supply current	A,B		16	21	mA	
Input bias current	A,B		7	25	μA	
Input offset voltage	A,B			5	mV	
Dynamic open loop gain	A	45	54		dB	600Ω load
	B	60	71		dB	
Open loop temperature coefficient	A,B		-0.02		dB/° C	
Closed loop bandwidth (-3dB)	A,B		100		MHz	X10 gain
Slew rate (4V peak)	A,B	100	175		V/μs	X10 gain
Settling time to 1 %	A,B		50	100	ns	
Maximum output voltage						
(+ve)	A	5.5	5.7		V	
(-ve)	A		-1.9	-1.5	V	
(+ve)	B	2.5	3.0		V	
(-ve)	B		-3.0	-2.5	V	
Maximum output current	A,B	4	6.5		mA	
Maximum input voltage						
(+ve)	A			5	V	
(-ve)	A	-1			V	Non-inverting
(+ve)	B			3	V	modes
(-ve)	B	-3			V	
Supply line rejection						
(+ve)	A,B	54	66		dB	
(-ve)	A,B	46	54		dB	
Input offset current	A,B			9.85	μA	
Common mode rejection	A,B	60.7			dB	
Input offset voltage drift	A		25		μV/° C	

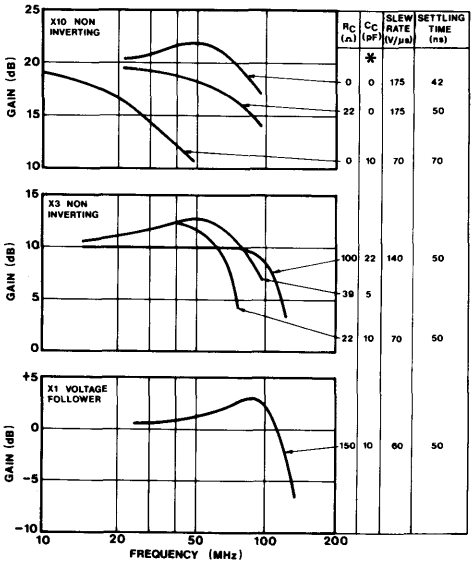


*Fig. 3 Performance graphs – gain v. frequency (load = 2kΩ/10pF) * See operating note 2*

OPERATING NOTES

The SL541 may be used as a normal, but non saturating operational amplifier, in any of the usual configurations (amplifiers, integrators etc.), provided that the following points are observed:

1. Positive supply line decoupling back to the output load earth should always be provided close to the device terminals.
2. Compensation capacitors should be connected between pins 4 and 5. These may have any value greater than that necessary for stability without causing side offsets.
3. The circuit is generally intended to be fed from a fairly low impedance (<1kΩ), as seen from pins 6 and 9 – 100Ω or less results in optimum speed.
4. The circuit is designed to withstand a certain degree of capacitive loading (up to 20pF) with virtually no effect. However, very high capacitive loads will cause loss of speed due to the extra compensation required and asymmetric output slew rates.
5. Pin 10 does not need to be connected to zero volts except where the clipping levels need to be defined accurately w.r.t. zero. If disconnected, an extra ±0.5 volt uncertainty in the clipping levels results, but the separation remains. However, the supply line rejection is improved if pin 10 can be left open-circuit (circuit B only).

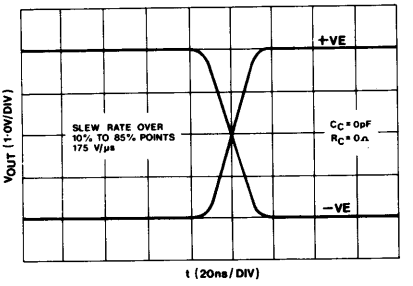


Fig. 4 Slew rate – X10 non-inverting mode Input square wave 0.4V p/p

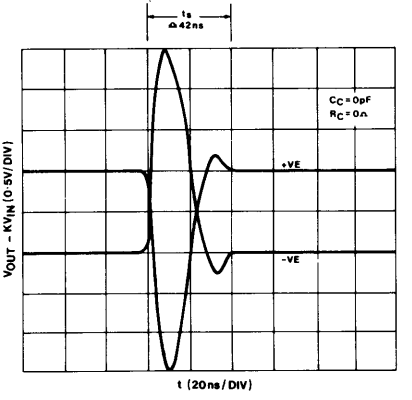


Fig. 5 Settling time – X10 non-inverting mode

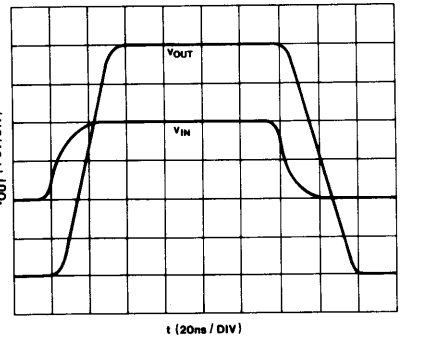


Fig. 6 Output clipping levels – X10 non-inverting mode Input moderately overdriven, so that ouput goes into clipping both sides

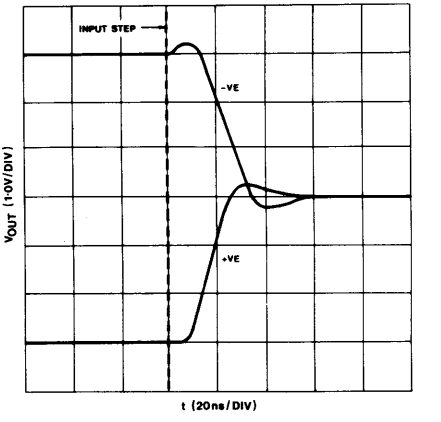


Fig. 7 Output clippings levels -X10 non inverting mode. Output goes from clipping to zero volts. $V_{in} = 3V$ peak step, offset +ve or – ve.

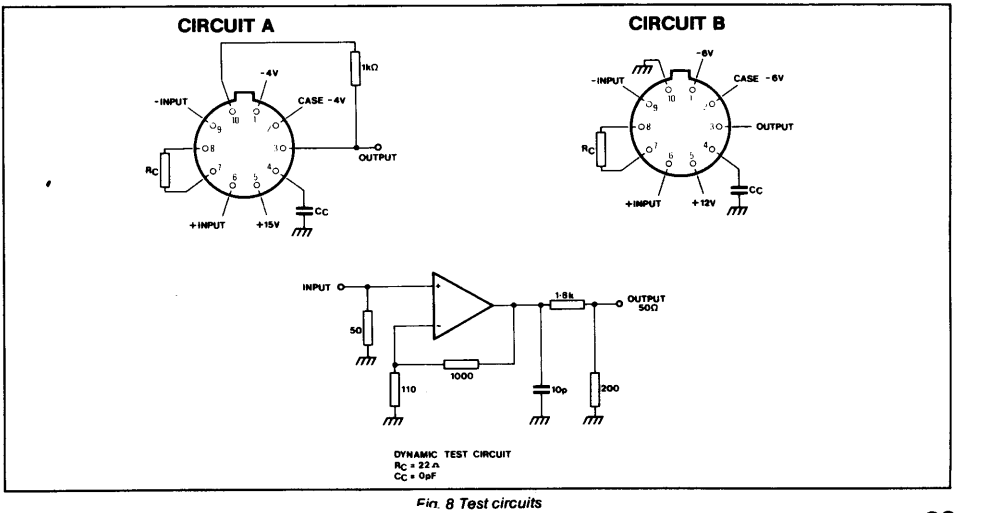


Fig. 8 Test circuits

TEST CONDITIONS AND DEFINITIONS

Both slew rate and settling time are measures of an amplifier's speed of response to an input. Slew rate is an inherent characteristic of the amplifier and is generally less subject to misinterpretation than is settling time, which is often more dependent upon the test circuit than the amplifier's ability to perform.

Slew rate defines the maximum rate of change of output voltage for a large step input change and is related to the full power frequency response (fp) by the relationship.

$$S = 2\pi f_p E_o$$

where E_o is the peak output voltage

Settling time is defined as the time elapsed from the application of a fast input step to the time when the amplifier output has entered and remained within a specified error band that is symmetrical about the final value. Settling time, therefore, is comprised of an initial propagation delay, an additional time for the amplifier to slew to the vincinity of some value of output voltage, plus a period to recover from overload and settle within the given error band.

The SL541 is tested for slew rate in a X10 gain configuration.

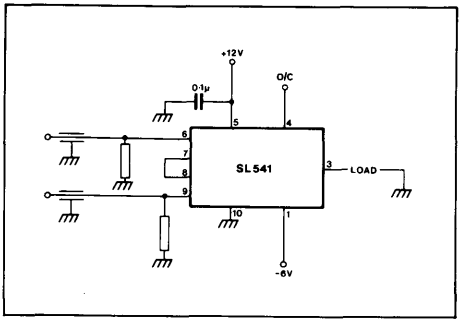


Fig. 9 Non-saturating sense amplifier (30V/μs for 5mV) Note: the output may be caught at a pre-determined level. (TO-5 pin nos.)

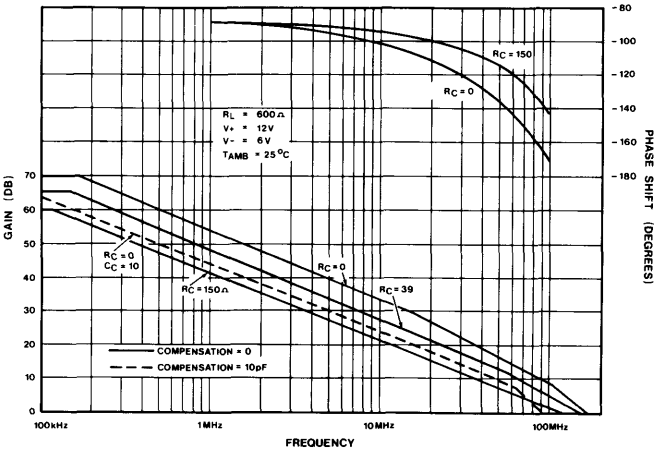


Fig.10 SL541B open loop gain and phase shift v. frequency

PLESSEY
Semiconductors

SL550 D & G

LOW NOISE WIDEBAND AMPLIFIER WITH EXTERNAL GAIN CONTROL

The SL550 is a silicon integrated circuit designed for use as a general-purpose wideband linear amplifier with remote gain control. At a frequency of 60 MHz, the SL550C noise figure is 1·8dB (typ.) from a 200 ohm source, giving good noise performance directly from a microwave mixer. The SL550 has an external gain control facility which can be used to obtain a swept gain function and makes the amplifier ideal for use either in a linear IF strip or as a low noise preamplifier in a logarithmic strip.

External gain control is performed in the feedback loop of the main amplifier which is buffered on the input and output, hence the noise figure and output voltage swing are only slightly degraded as the gain is reduced. The external gain control characteristic is specified with an accuracy of ±1dB, enabling a well-defined gain versus time law to be obtained.

The input transistor can be connected in common emitter or common base and the quiescent current of the output emitter follower can be increased to enable low impedance loads to be driven.

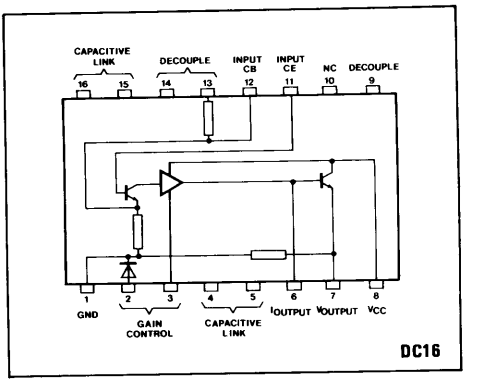


Fig. 1 Pin connections (top view)

FEATURES

- 200 MHz Bandwidth
- Low Noise Figure
- Well-Defined Gain Control Characteristic
- 25dB Gain Control Range
- 40dB Gain
- Output Voltage 0.8Vp-p (Typ.)

APPLICATIONS

- Low Noise Preamplifiers
- Swept Gain Radar IFs

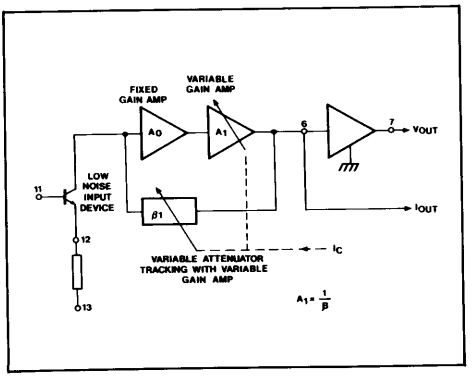


Fig. 2 Functional diagram

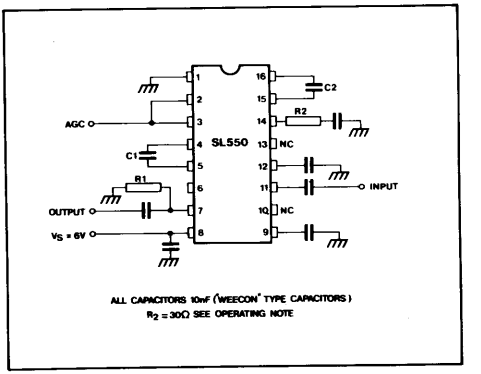


Fig. 3 Test circuit

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
f = 30Hz V_S = +6V, R_L = 200Ω, I_C = O, R_1 = 750Ω, T_{amb} = +25°C

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Voltage gain	SL550G	39	42	44	dB	
	SL550D	35	40	45	dB	
Gain control characteristic	Both		See note 1			
Gain reduction at mid-point	SL550G		10		dB	I_C = 0.24mA
	SL550D		9		dB	I_C = 0.2mA
Max. gain reduction	SL550G	20	25		dB	I_C = 2.0mA
	SL550D		25		dB	I_C = 2.0mA
Noise figure	SL550G		2.0	2.7	dB	R_S = 200Ω
	SL550G		3.5		dB	R_S = 50Ω
	SL550D		3.0		dB	R_S = 200Ω
Output voltage	Both		0.15		Vrms	R_1 = ∞
	Both		0.3		Vrms	R_1 = 750Ω
Supply current	SL550G		11	13	mA	R_1 = ∞
	SL550G		15		mA	R_1 = 750Ω
	SL550D		11	20	mA	R_1 = ∞
Gain variation with supply voltage	Both		0.2		dB/V	V_S = 6 to 9V
Upper cut-off frequency (—3dB wrt 30MHz)	Both		125		MHz	
Gain variation with temperature (see note 2)	Both		±3		dB	T_{amb} = —55 to +125°C

NOTES
1. The external gain control characteristic is specified in terms of the gain reduction obtained when the control current (I_C) is increased from zero to the specified current.
2. This can be reduced by using an alternative input configuration (see operating note: 'Wide Temperature Range').

OPERATING NOTES

Input Impedance

The input capacitance, which is typically 12pF at 60MHz, is independent of frequency. The input resistance, which is approximately 1.5k at 10MHz, decreases with frequency and is typically 500 ohms at 60MHz.

Control Input

Gain control is normally achieved by a current into pin 2. Between pin 2 and ground is a forward biased diode and so the voltage on pin 2 will vary between 600 mV at I_C = 1µA to 800 mV at I_C = 2 mA. The amplifier gain is varied by applying a voltage in this range to pin 3. To avoid problems associated with the sensitivity of the control voltage and with operation over a wide temperature range the diode should be used to convert a control current to a voltage which is applied to pin 3 by linking pins 2 and 3.

Minimum Supply Current

If the full output swing is not required, or if high impedance loads are being driven, the current consumption can be reduced by omitting R_1 (Fig. 3). The function of R_1 is to increase the quiescent current of the output emitter follower.

High Output Impedance

A high impedance current output can be obtained by taking the output from pin 6 (leaving pin 7 open-circuit). Maximum output current is 2 mA peak and the output impedance is 350Ω.

Wide Temperature Range

The gain variation with temperature can be reduced at the expense of noise figure by including an internal 30Ω resistor in the emitter of the input transistor. This is achieved by decoupling pin 13 and leaving pin 12 open-circuit. Gain variation is reduced from ±3dB to ±1dB over the temperature range —55°C to +125°C (Figs. 6 and 7).

Low Input Impedance

A low input impedance (≃25Ω) can be obtained by connecting the input transistor in common base. This is achieved by decoupling pin 11 and applying the input to pin 12 (pin 13 open-circuit).

High Frequency Stability

Care must be taken to keep all capacitor leads short and a ground plane should be used to prevent any earth inductance common between the input and output circuits. The 30Ω resistor (pin 14) shown in the test circuit eliminates high frequency instabilities due to the stray capacitances and inductances which are unavoidable in a plug-in test system. If the amplifier is soldered directly into a printed circuit board then the 30Ω resistor can be reduced or omitted completely.

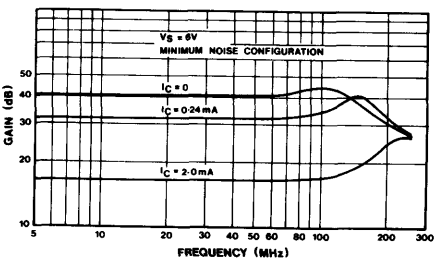


Fig. 4 Frequency response

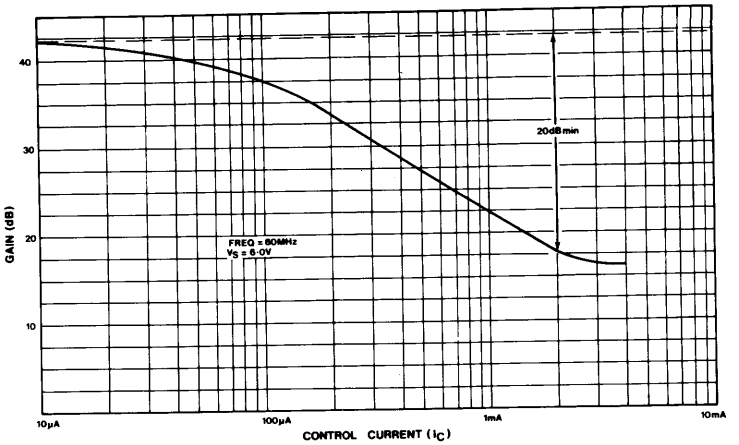


Fig. 5 Gain control characteristic

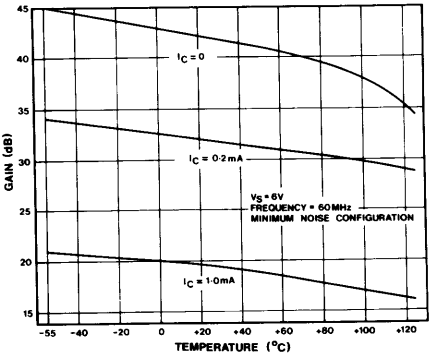


Fig. 6 Voltage gain v. temperature (pin 12 decoupled, standard circuit configuration)

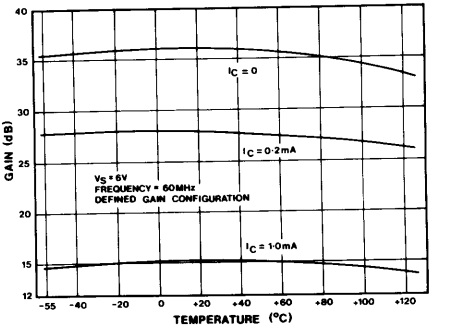


Fig. 7 Voltage gain v. temperature (pin 13 decoupled for improved gain variation with temperature – see operating notes)

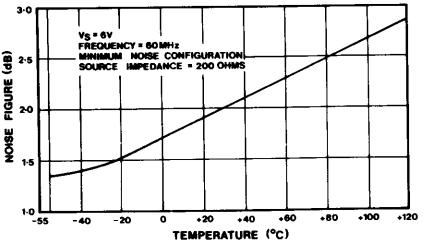


Fig. 8 Typical noise figure (SL550G)

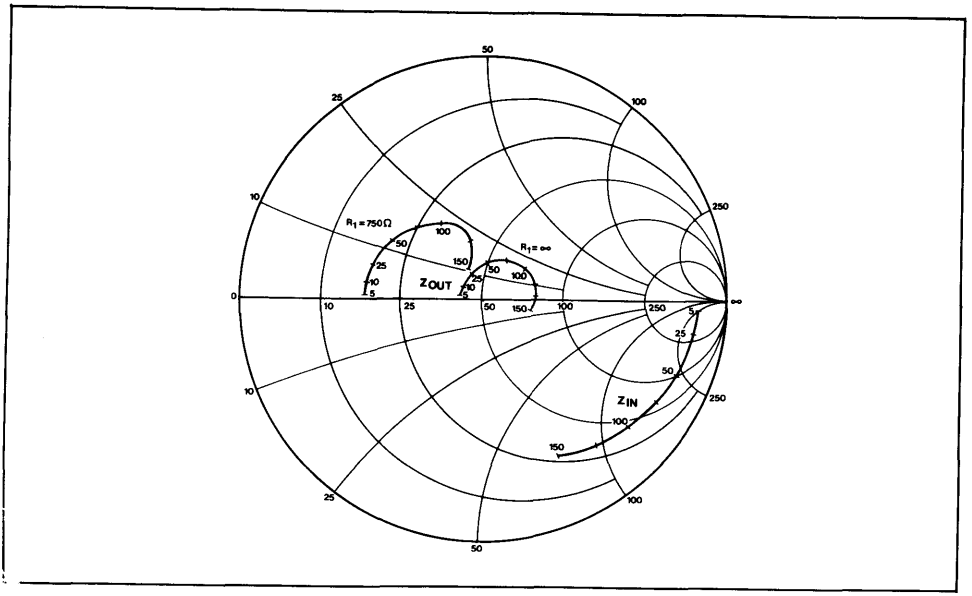


Fig. 9 Input and output impedances (V_S = 6V)

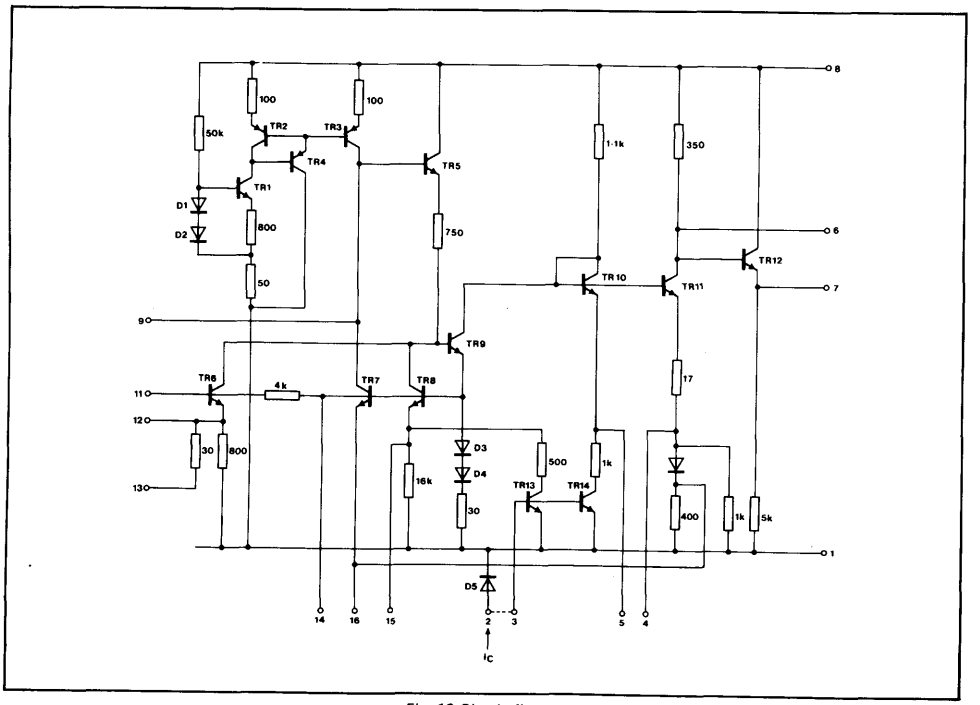


Fig. 10 Circuit diagram

APPLICATION NOTES

A wideband high gain configuration using two SL550s connected in series is shown in Fig. 11. The first stage is connected in common emitter configuration, whilst the second stage is a common base circuit. Stable gains of up to 65 dB can be achieved by the proper choice of R1 and R2. The bandwidth is 5 to 130 MHz, with a noise figure only marginally greater than the 2.0 dB specified for a single stage circuit.

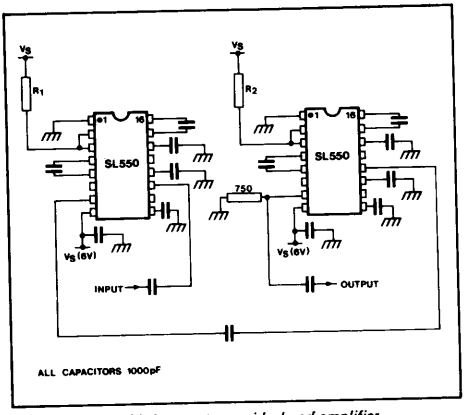


Fig. 11 A two-stage wide-band amplifier

A voltage gain control which is linear with control voltage can be obtained using the circuit shown in Fig. 12. The input is a voltage ramp which is negative going with respect to ground. The output drives the control current pins 2 and 3 directly (see Fig. 13). If two SL550s in the strip are controlled as shown in Fig. 14, with a linear ramp input to the linearising circuit, a fourth power law (power gain v. time) will be obtained over a 50 dB dynamic range.

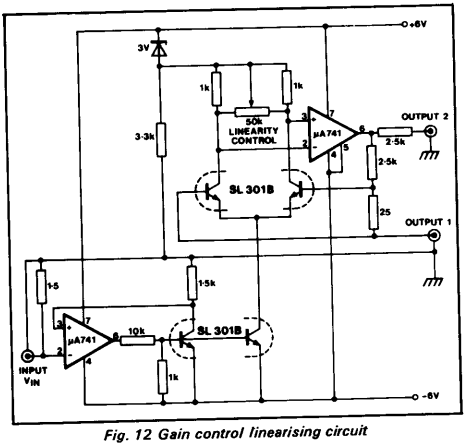


Fig. 12 Gain control linearising circuit

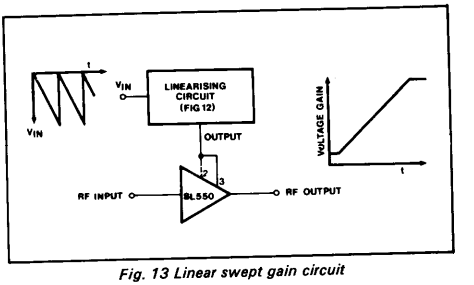


Fig. 13 Linear swept gain circuit

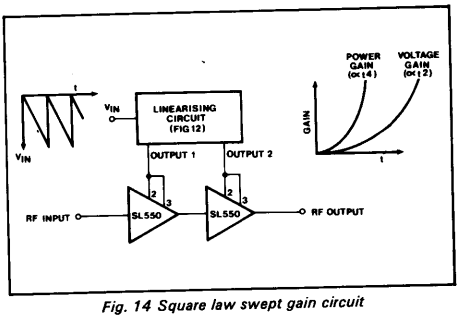
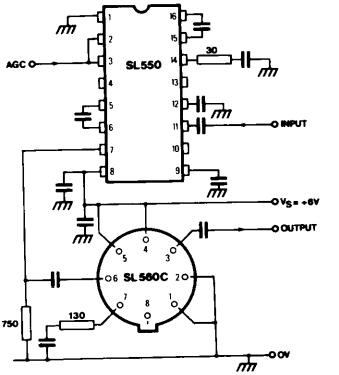


Fig. 14 Square law swept gain circuit



All Capacitors 10nF
Gain 46dB
Noise figure 2.0dB (RS = 200Ω)
Output power +5dBm (R1 = 50Ω)
Frequency response as SL550G
Dynamic range 70dB (1MHz bandwidth)

Fig. 15 Applications example of wide dynamic range: 50Ω load amplifier with AGC using SL500 series integrated circuit.

ABSOLUTE MAXIMUM RATINGS

Storage temperature	—55°C to +150°C
Ambient operating temp.	—40°C to +125°C
Max. continuous supply Voltage wrt pin 1	+9V
Max. continuous AGC current pin 2	10mA
pin 3	1mA

PLESSEY
Semiconductors

SL560C

300 MHz LOW NOISE AMPLIFIER

This monolithic integrated circuit contains three very high performance transistors and associated biasing components in an eight-lead TO-5 package forming a 300 MHz low noise amplifier. The configuration employed permits maximum flexibility with minimum use of external components. The SL 560C is a general-purpose low noise, high frequency gain block.

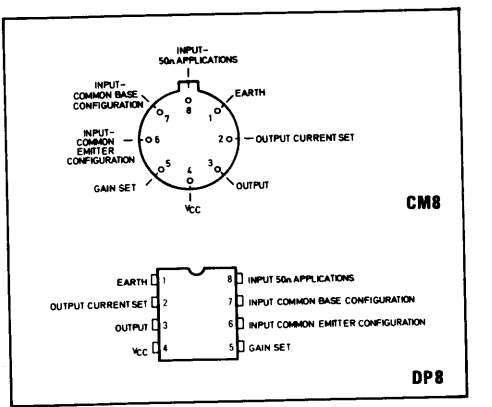


Fig. 1 Pin connections (viewed from beneath)

FEATURES
(Non-simultaneous)

- Gain up to 40 dB
- Noise Figure Less Than 2 dB (R_S 200 ohm)
- Bandwidth 300 MHz
- Supply Voltage 2-15V (Depending on Configuration)
- Low Power Consumption

APPLICATIONS

- Radar IF Preamplifiers
- Infra-Red Systems Head Amplifiers
- Amplifiers in Noise Measurement Systems
- Low Power Wideband Amplifiers
- Instrumentation Preamplifiers
- 50 ohm Line Drivers
- Wideband Power Amplifiers
- Wide Dynamic Range RF Amplifiers
- Aerial Preamplifiers for VHF TV and FM Radio

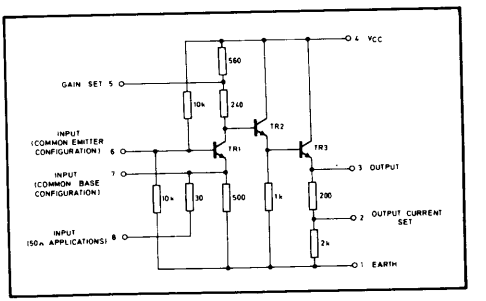


Fig. 2 SL560C circuit diagram

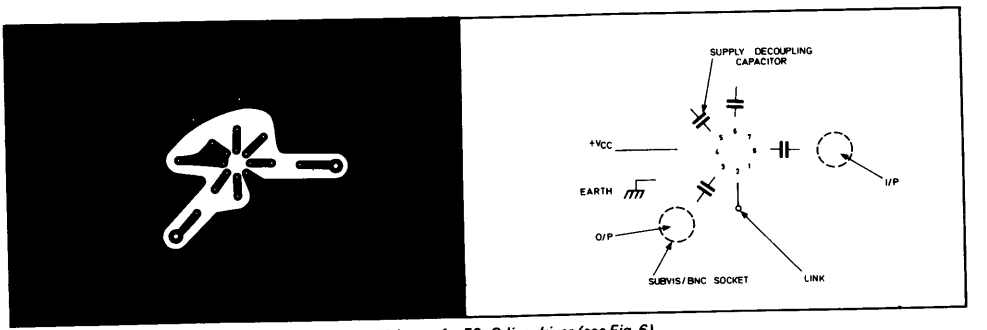


Fig. 3 PC layout for 50- Ω line driver (see Fig. 6)

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Frequency 30 MHz
V_{CC} 6V
$R_S = R_L = 50\Omega$
$T_A = 25°C$
Test Circuit: Fig. 6

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Small signal voltage gain	11	14	17	dB	
Gain flatness		±1.5		dB	10 MHz — 220 MHz
Upper cut-off frequency		250		MHz	
Output swing	+5	+7		dBm	V_{CC} = 6V } See Fig. 5
		+11		dBm	V_{CC} = 9V }
Noise figure (common emitter)		1.8		dB	$R_S = 200\Omega$
		3.5		dB	$R_S = 50\Omega$
Supply current		20	30	mA	

CIRCUIT DESCRIPTION

Three high performance transistors of identical geometry are employed. Advanced design and processing techniques enable these devices to combine a low base resistance ($R_{bb'}$) of 17 ohms (for low noise operation) with a small physical size — giving a transition frequency, f_T, in excess of 1 GHz.

The input transistor (TR1) is normally operated in common base, giving a well defined low input impedance. The full voltage gain is produced by this transistor and the output voltage produced at its collector is buffered by the two emitter followers (TR2 and TR3). To obtain maximum bandwidth the capacitance at the collector of TR1 must be minimised. Hence, to avoid bonding pad and can capacitances, this point is not brought out of the package. The collector load resistance of TR1 is split, the tapping being accessible via pin 5. If required, an external roll-off capacitor can be fixed to this point.

The large number of circuit nodes accessible from the outside of the package affords great flexibility, enabling the operating currents and circuit configuration to be optimised for any application. In particular, the input transistor (TR1) can be operated in common emitter mode by decoupling pin 7 and using 6 as the input. In this configuration, a 2 dB noise figure ($R_S = 200\ \Omega$) can be achieved. This configuration can give a gain of 35dB with a bandwidth of 75 MHz (see Figs. 8 and 9) or, using feedback, 14 dB with a bandwidth of 300 MHz (see Figs. 10 and 11).

Because the transistors used in the SL 560C exhibit a high value of f_T, care must be taken to avoid high frequency instability. Capacitors of small physical size should be used, the leads of which must be as short as possible to avoid oscillation brought about by stray inductance. The use of a ground plane is recommended.

Further applications information is avaiable in the 'Broadband Amplifier Applications' booklet.

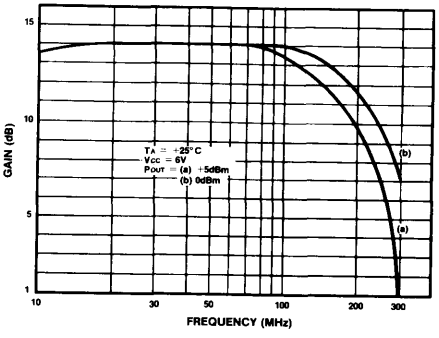


Fig. 4 Frequency response, small signal gain

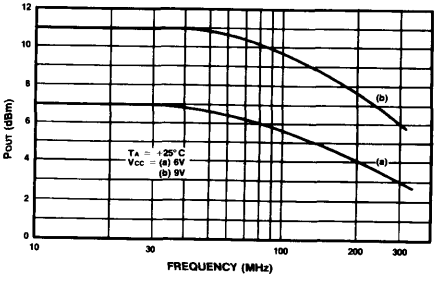


Fig. 5 Frequency response, output capability (loci of maximum output power with frequency, for 1dB gain compression)

TYPICAL APPLICATIONS

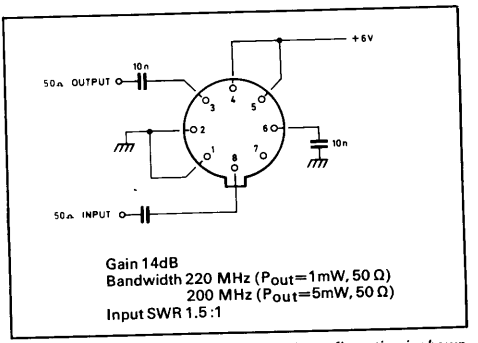


Fig. 6 50 Ω line driver. The response of this configuration is shown in Fig. 4.

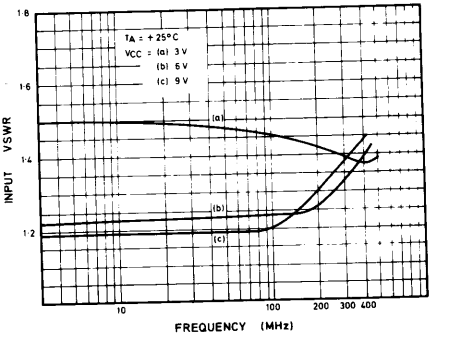


Fig. 7 Input standing wave ratio plot of circuit shown in Fig. 6

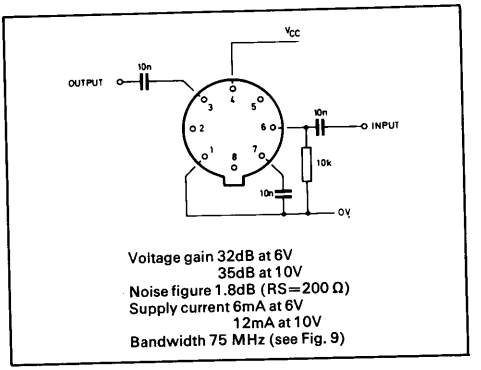


Fig. 8 Low noise preamplifier

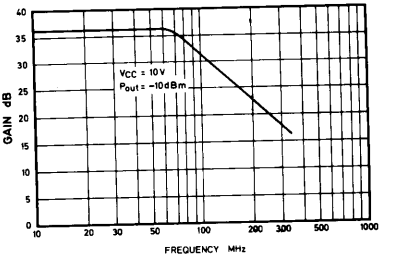


Fig. 9 Frequency response of circuit shown in Fig. 8

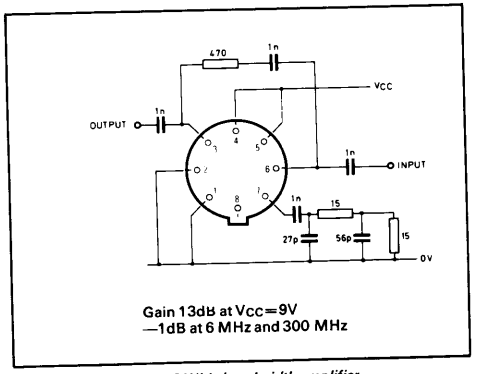


Fig. 10 Wide bandwidth amplifier

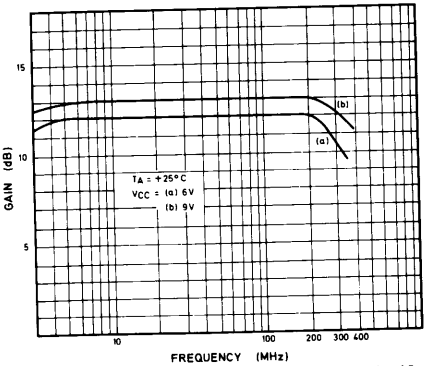


Fig. 11 Frequency response of circuit shown in Fig. 10

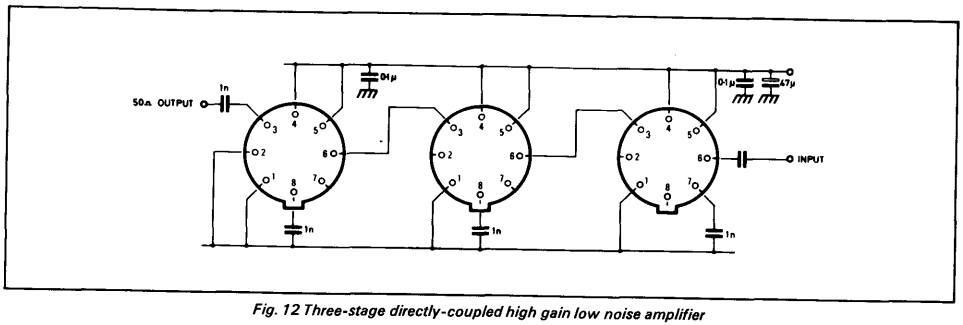


Fig. 12 Three-stage directly-coupled high gain low noise amplifier

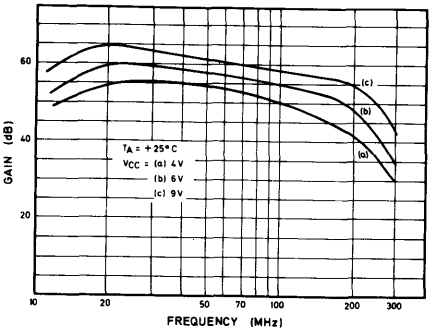


Fig. 13 Frequency response of circuit shown in Fig. 12

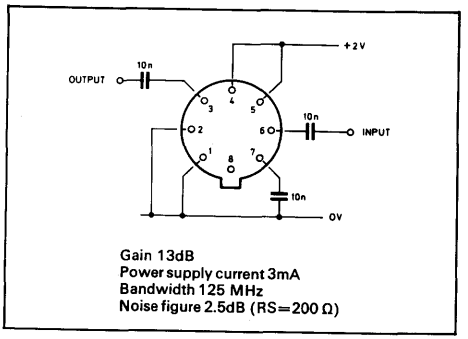


Fig. 14 Low power consumption amplifier

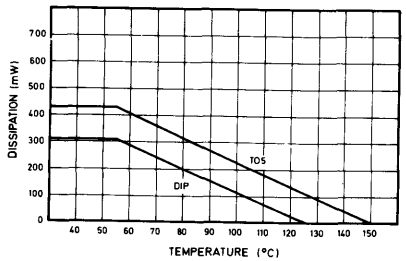


Fig. 15 Ambient operating temperature v. degrees centigrade

ABSOLUTE MAXIMUM RATINGS

Supply voltage (Pin 4)	+15V
Storage temperature	−55°C to 150°C (CM)
	−55°C to 125°C (DP)
Junction temperature	150°C (TO5) 125°C (DIP)
Thermal resistance	
Junction-case	60°C/W (TO5)
Junction ambient	220°C/W (T05) 230°C/W (DIP)
Maximum power dissipation	See Fig. 15
Operating temperature range	−55°C to +125°C (TO5) at 100 mW
	−55°C to +100°C (DIP) at 100 mW

PLESSEY
Semiconductors

SL561C

ULTRA LOW NOISE PREAMPLIFIERS

This integrated circuit is a high gain, low noise preamplifier designed for use in audio and video systems at frequencies up to 6MHz. Operation at low frequencies is eased by the small size of the external components and the low 1/*f* noise. Noise performance is optimised for source impedances between 20Ω and 1kΩ making the device suitable for use with a number of transducers including photo-conductive IR detectors, magnetic tape heads and dynamic microphones.

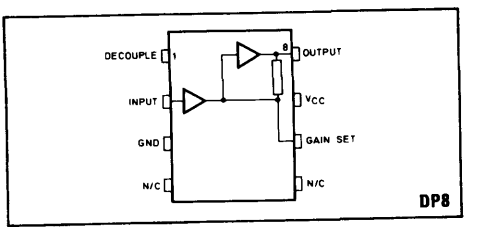


Fig. 1 Pin connections (viewed from the top)

APPLICATIONS

- Audio Preamplifiers (low noise from low impedance source)
- Video Preamplifier
- Preamplifier for use in Low Cost Infra-Red Systems

FEATURES

- High Gain 60dB
- Low noise 0.8nV/√Hz (Rs = 50Ω)
- Bandwidth 6MHz
- Low Power Consumption 10mW (Vcc = 5V)

ABSOLUTE MAXIMUM RATINGS

Supply voltage 10V
Storage temperature −55°C to +125°C
Operating temperature −55°C to +100°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Vcc 5V
Source impedance 50Ω
Load impedance 10kΩ
T_{amb} 25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	57	60	63	dB	Pin 6 0/C
Equivalent input noise voltage		0.8		nV√Hz	100Hz to 6MHz
Input resistance		3		kΩ	
Input capacitance		15		pF	
Output impedance		50		Ω	
Output voltage	2	3		V p-p	See note 4
Supply current		2	3	mA	
Bandwidth		6		MHz	

OPERATING NOTES

1. Upper cut-off frequency

The bandwidth of the amplifier can be reduced from 6MHz to any desired value by a capacitor from pin 6 to ground. This is shown in Fig. 5. No degradation in noise or output swing occurs when this capacitor is used. The high frequency roll off is approximately 6dB/ octave.

2. Low frequency reponse

The capacitors C_2 and C_3 (Fig. 4) determine the lower cut-off frequency. C_2 decouples an internal feedback loop and if its value is close to that of C_3 an increase in gain at low frequencies can occur. For a flat response either make C2 less than 0.05 C3 or make C2 greater than 5 C1.

3. Gain set facility

Provision is made to adjust the gain by means of a resistor between pin 6 and the output. Gains as low as 10dB can be selected. This resistor increases the feedback around the output stage and stability problems can result if the bandwidth of the amplifier is not reduced as indicated in Note 1. Fig.6 shows recommended values of C_1 for each gain range. Since the input stage is a common emitter stage without emitter degeneration (for best noise) at values of gain less than 40dB this input stage, rather than the output stage, determines the maximum output voltage swing. For a distortion of less than 10% the input voltage should be restricted to less than 5mV.

4. Driving low impedance loads

The quiescent current of the output emitter follower is 0.5mA. If larger voltage swings are required into low impedance loads this current can be increased by a resistor from pin 8 to ground. To avoid exceeding the ratings of the output transistor the resistor should not be less than 200Ω.

5. Noise performance

The equivalent input voltage for the amplifier is shown in Fig.7. From this the input noise voltage and current generators can be derived. They are :-

$e_n = 0.8nV/\sqrt{Hz}$

$i_n = 2.0pA/\sqrt{Hz}$

Flicker or **1/f** noise is not normally a problem, the knee frequency being typically below 100Hz.

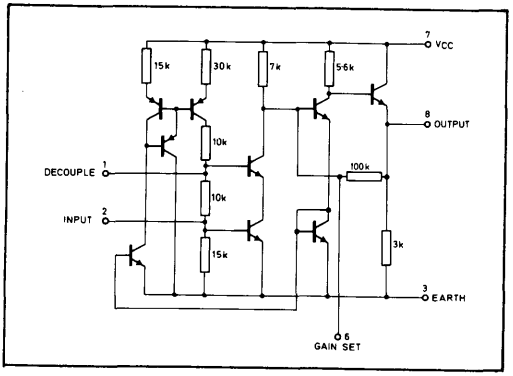


Fig. 2 Circuit diagram

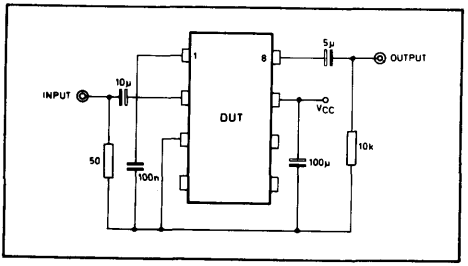


Fig. 3 Test circuit

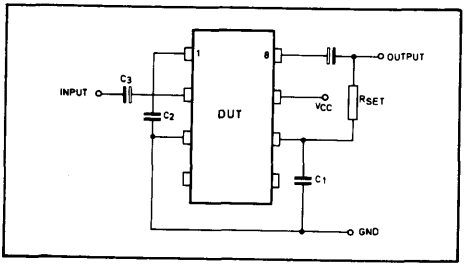


Fig. 4 Typical application

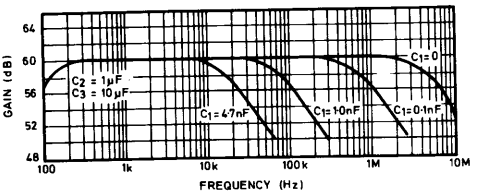


Fig. 5 Gain v. frequency

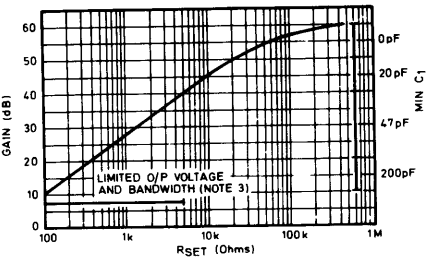


Fig. 6 Gain v. R_{set}

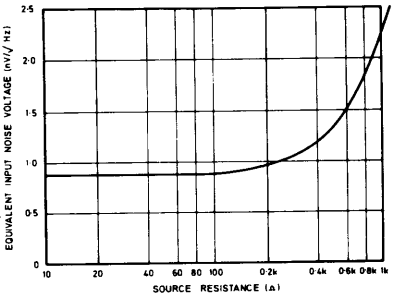


Fig. 7 Noise v. source impedance

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ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

SL565C

1GHz WIDEBAND AMPLIFIER

The SL565 is a low cost wide bandwidth amplifier featuring differential inputs and outputs and useful performance to 1GHz. Typical applications are in wideband amplifiers, instrumentation, ECM and communications.

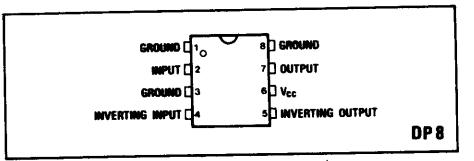

Fig.1 Pin connections - top view

FEATURES

- Low Cost
- Wide Bandwidth: 1GHz
- High Gain: 22dB
- Differential Input and Output
- +5V Supply
- High Reverse Isolation

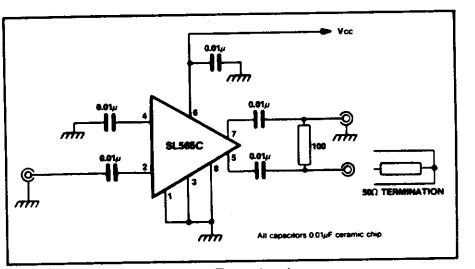

Fig.2 Test circuit

ABSOLUTE MAXIMUM RATINGS

Supply voltage, Vcc +8V
Storage temperature -55°C to +125°C
Operating temperature -30°C to +85°C
Chip temperature +150°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Vcc = 5.0V T_{amb} = +25°C. Test circuit Fig.2 except for differential gain measurements.

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply voltage	4.75	5.0	5.5	V	
Supply current	30	50	70	mA	
Differential gain S_{21}		16		dB	10-900MHz
		21		dB	1GHz
		16		dB	1.3GHz
Single ended gain	8	10	12		100MHz
	13	15	17		500MHz
	8	10	12		1GHz
1dB gain compression		-19		dBm	Input power at 500MHz
Noise figure		13		dB	50Ω source
3rd order input intercept point		-3.5		dBm	50MHz
		-7		dBm	200MHz
		-9.5		dBm	500MHz
2nd order input intercept point		+3.0		dBm	500 and 400MHz inputs
Reverse isolation pins 7 to 4		70		dB	f = 50MHz
		60		dB	f = 50-100MHz
		20		dB	f = 500MHz
		20		dB	f = 1GHz
Reverse isolation pins 5 to 4		75		dB	f = 100MHz
		30		dB	f = 1GHz
Maximum output		600		mV p-p	f < 500MHz
		300		mV p-p	f = 500MHz to 1GHz
Maximum output power for 1dB compression		-3		dBm	1GHz
		-2		dBm	500MHz

OPERATING NOTES

The SL565 is a general purpose wideband gain block, suitable for many applications. The frequency response and input impedance plots are shown in Figs. 3 and 4 respectively.

Like all wideband high frequency circuits, the SL565 should be used with short leads to its associated components, and a ground plane printed circuit board layout is recommended. There are advantages in using the top surface of the PCB as the ground plane with cage jacks e.g. Cambion 450-3750-01-06-00 or similar sockets for each device pin, as then chip capacitors can be installed with minimum lead lengths on top of the board. Resistors should be miniature carbon composition types (metal oxide and carbon film types often have an appreciable parasitic inductance).

The high reverse isolation makes the SL565 ideal for driving High Speed Divider integrated circuits in both frequency counters and synthesisers, and Fig. 5 shows a typical application in a 100MHz to 1000MHz ÷10 prescaler for a frequency counter. This prescaler operates with inputs as low as 70mV rms over the whole frequency range of the device.

Other applications for the SL565 include oscillators using SAW devices as frequency determining elements, where the wide bandwidth of the SL565 enables high frequency oscillators to be produced at minimum cost.

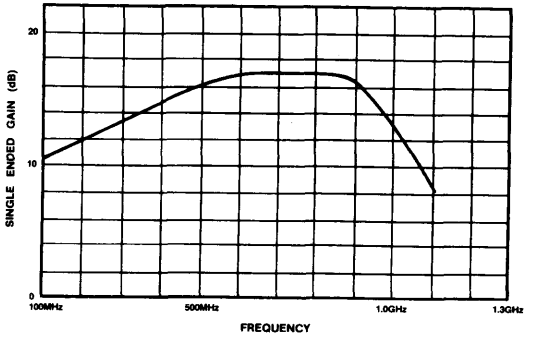

Fig.3 Typical frequency response, SL565C

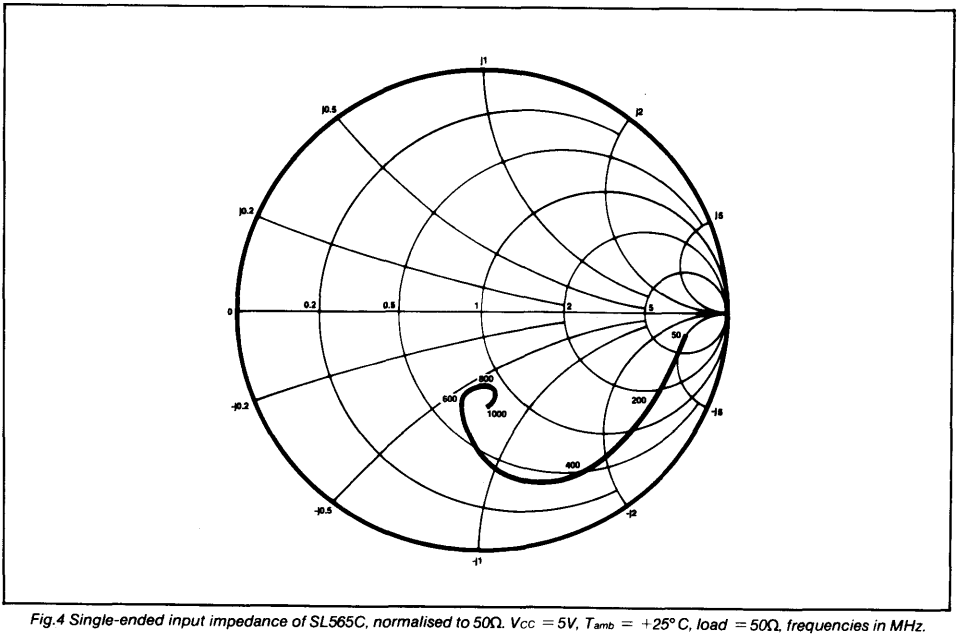

Fig.4 Single-ended input impedance of SL565C, normalised to 50Ω. V_{CC} = 5V, T_{amb} = +25°C, load = 50Ω, frequencies in MHz.

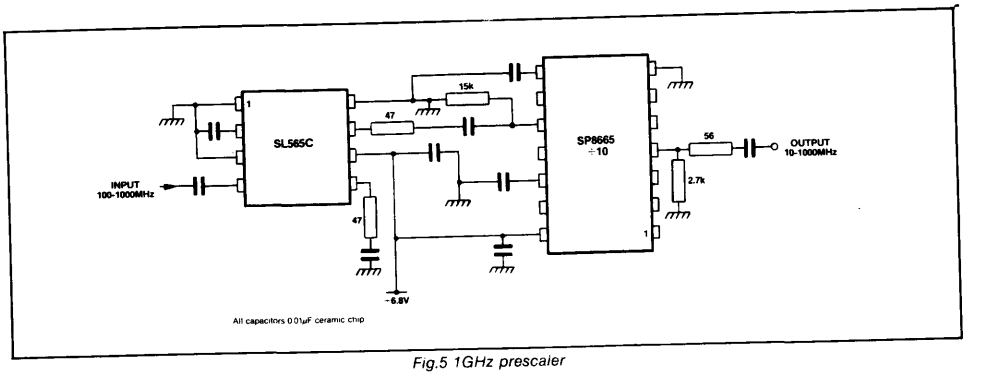

Fig.5 1GHz prescaler

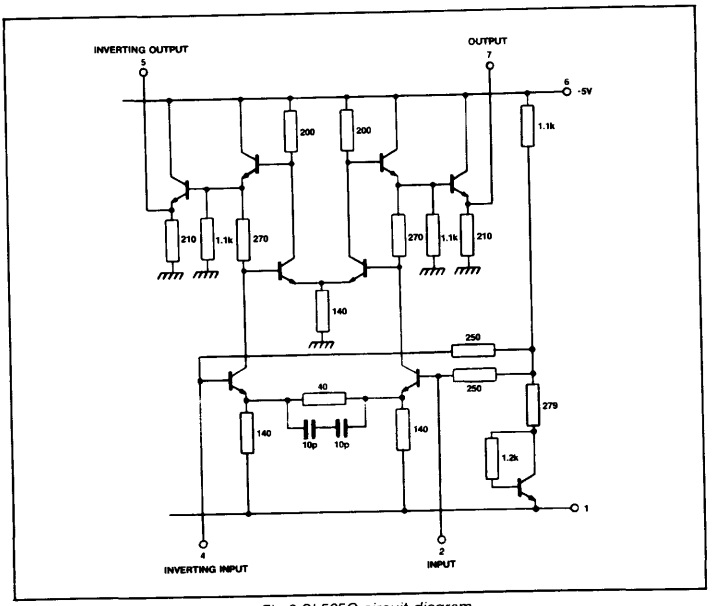

Fig.6 SL565C circuit diagram

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SL610C, SL611C & SL612C

RF/IF AMPLIFIERS

The SL610C, SL611C and SL612C are RF voltage amplifiers with AGC facilities. The voltage gains are 10, 20 and 50 times respectively and the upper frequency response varies from 15 MHz to 120 MHz according to type.

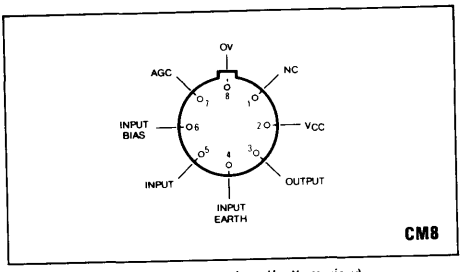

Fig. 1 Pin connections (bottom view)

FEATURES

- Wide AGC Range: 50dB
- Easy Interfacing
- Integral Power Supply RF Decoupling

APPLICATIONS

- RF Amplifiers
- IF Amplifiers

QUICK REFERENCE DATA

- Supply Voltage: 6V
- Voltage Gain: 20dB to 34dB

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: −55°C to +125°C

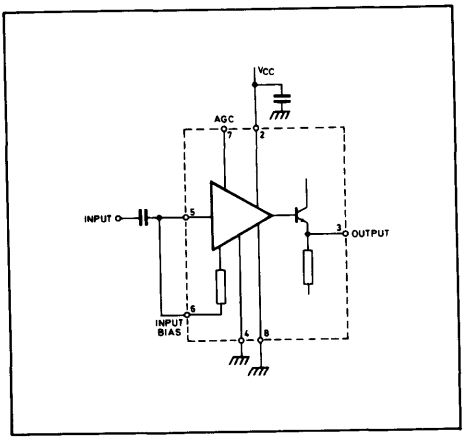

Fig. 2 Block diagram

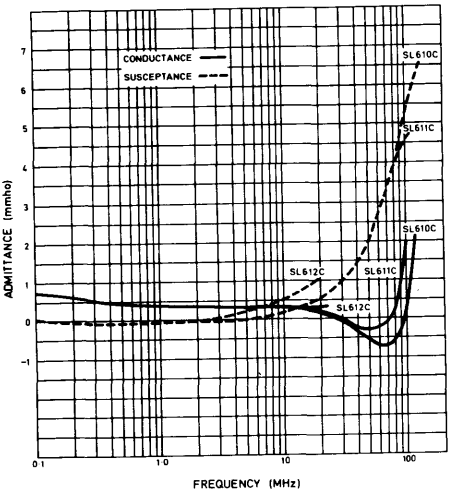

Fig. 3 Input admittance with o/c output (G_{11})

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage V_{CC}: 6V
Ambient temperature: −30°C to +85°C
Test frequency: SL610C 30MHz
SL611C 30MHz
SL612C 1.75MHz

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	SL610C		15	20	mA	No signal, pin 3 open circuit
	SL611C		15	20	mA	
	SL612C		3.3	5	mA	
Voltage gain	SL610C	18	20	22	dB	$R_S = 50\Omega$, $R_L = 500\Omega$, $T_{amb} = 22°C$
	SL611C	24	26	28	dB	
	SL612C	32	34	36	dB	
Cut-off frequency (−3dB)	SL610C	85	120		MHz	
	SL611C	50	80		MHz	
	SL612C	10	15		MHz	
Noise figure	SL610C		4		dB	$R_S = 300\Omega$ at test frequency
	SL611C		4		dB	$R_S = 300\Omega$ at test frequency
	SL612C		3		dB	$R_S = 800\Omega$ at test frequency
Max. output signal (max. AGC)			1.0		Vrms	$R_L = 150\Omega$ (SL610C/611C), $R_L = 1.2k\Omega$ (SL612C)
Max. input signal (max. AGC)			250		mVrms	
AGC range	SL610C	40	50		dB	Pin 7 0V to 5.1V
	SL611C	40	50		dB	
	SL612C	60	70		dB	
AGC current			0.15	0.6	mA	Current into pin 7 at 5.1V

APPLICATION NOTES

Input circuit

The SL610C, SL611C and SL612C are normally used with pins 5 and 6 connected together and with the input connected via a capacitor as shown in Fig. 2.

The input impedance is negative between 30MHz and 100MHz (SL610C, SL611C only) and is shown in Fig. 3. If the source is inductive it should be shunted by a 1kΩ resistor to prevent oscillation.

An alternative input circuit with improved noise figure is shown in Fig. 4.

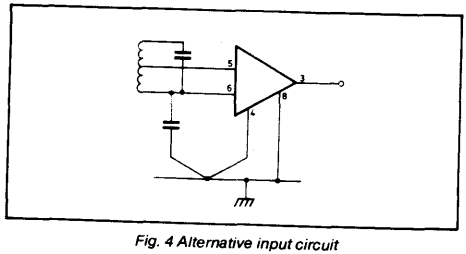

Fig. 4 Alternative input circuit

Output circuit

The output stage is an emitter follower and has a negative output impedance at certain frequencies as shown in Fig. 5.

To prevent oscillation when the load is capacitive a 47Ω resistor should be connected in series with the output.

AGC

When pin 7 is open circuit or connected to a voltage less than 2V the voltage gain is normal. As the AGC voltage is increased there is a reduction in gain as shown in Fig. 6. This reduction varies a little with temperature.

Typical applications

The circuit of Fig. 7 is a general purpose RF preamplifier. The voltage gain (from pin 5 to pin 3) is shown in Fig. 8. Fig. 9 is the IF section of a simple SSB transceiver. At 9MHz it has a gain of 100dB.

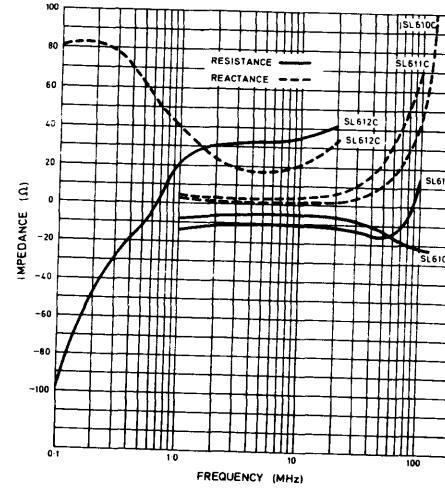

Fig. 5 Typical output impedance with s/c input (G22)

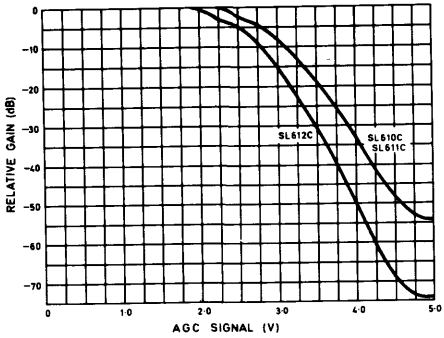

Fig. 6 AGC characteristics (typical)

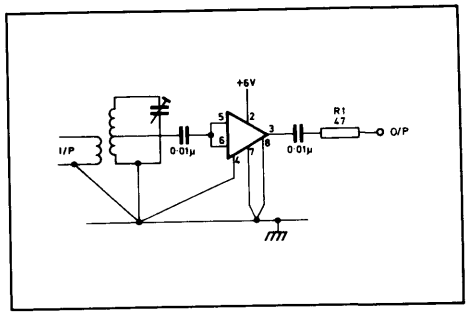

Fig. 7 RF preamplifier

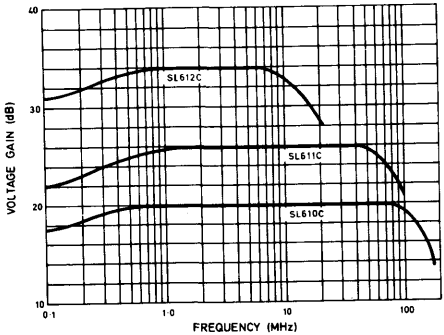

Fig. 8 Typical voltage gain (R_S=50 Ω)

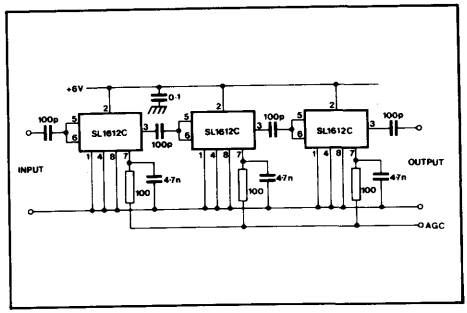

Fig. 9 IF amplifier using SL612

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SL621C

AGC GENERATOR

The SL621C is an AGC generator designed specifically for use in SSB receivers in conjunction with the SL610C, SL611C and SL612C RF and IF amplifiers. In common with other advanced systems it generates a suitable AGC voltage directly from the detected audio waveform, provides a 'hold' period to maintain the AGC level during pauses in speech, and is immune to noise interference. In addition it will smoothly follow the fading signals characteristic of HF communication.

When used in a receiver comprising one SL610C and one SL612C amplifier and a suitable detector, the SL621C will maintain the output within a 4dB range for a 110dB range of receiver input signal.

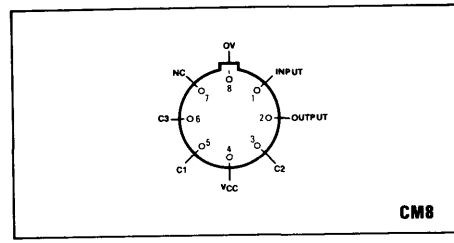

Fig. 1 Pin connections (bottom view)

FEATURES

- All Time Constants Set Externally
- Easy Interfacing
- Compatible with SL610/611/612

APPLICATIONS

- SSB Receivers
- Test Equipment

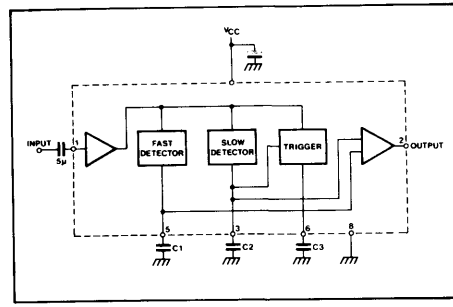

Fig. 2 Block diagram

QUICK REFERENCE DATA

- Supply voltage: 6V
- Supply current: 3mA

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC} = 6V
Ambient temperature: −30°C to +85°C
Test frequency: 1kHz
Test circuit as Fig. 2

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: −55°C to +125°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.1	4.3	mA	No signal
Cut-off frequency (−3dB)		6		kHz	
Input for 2.2V DC output	3	7	11	mVrms	
Input for 4.6V DC output	9	11	16	mVrms	
Maximum output voltage	5.1			V	
AC ripple on output		12	20	mV pk-pk	1kHz, output open circuit
Input resistance	350	500	700	Ω	
Output resistance		70	230	Ω	
'Fast' rise time t_1		20	55	ms	0 to 50% full output
'Fast' decay time t_2	150	200	330	ms	100% to 36% full output
'Slow' rise time t_3	150	200	300	ms	Time to output transistion point
Hold collapse time t_4	65	100	150	ms	90% to 10% full output
Hold time t_5	0.75	1.0	1.25	s	

APPLICATION NOTES

The SL621C consists of an input AF amplifier coupled to a DC output amplifier by means of two detectors having short and long rise and fall times respectively. The time constants of these detectors are set externally by capacitors on pins 5 (C_1) and 3 (C_2).

The detected audio signal at the input will rapidly establish an AGC level via the 'fast' detector time in t_1 (see Fig. 3). Meanwhile the long time constant detector output will rise and after t_3 will control the output because this detector is more sensitive.

Input signals greater than approximately 4mV rms will actuate a trigger circuit whose output pulses provide a discharge current for C_2.

By this means the voltage on C_2 can decay at a maximum rate, which corresponds to a rise in receiver gain of 20dB/s. Therefore the AGC system will smoothly follow signals which are fading at this rate or slower. However should the receiver input signals fade faster than this, or disappear completely as during pauses in speech, then the input to the AGC generator will drop below the 4mV rms threshold and the trigger will cease to operate. As C_2 then has no discharge path, it will hold its charge (and hence the output AGC level) at the last attained value. The output of the short time constant detector will drop to zero in time t_2 after the disappearance of the signal.

The trigger pulses also charge C_3. When the trigger pulses cease, C_3 discharges and after t_5 C_2 is discharged rapidly (in time t_4) and so full receiver gain is restored. The hold time, t_5 is approximately one second with $C_3 = 100\mu F$. If signals reappear during t_5, then C_3 will recharge and normal operation will continue. The C_3 recharge time is made long enough to prevent prolongation of the hold time by noise pulses.

Fig. 3 shows how a noise burst superimposed on speech will initiate rapid AGC action via the short time constant detector while the long time constant detector effectively remembers the pre-noise AGC level.

The various time constants quoted are for $C_1 = 50\mu F$ and $C_2 = C_3 = 100\mu F$. These time constants may be altered by varying the appropriate capacitors. C_1 controls t_1, t_2; C_2 controls t_3, t_4; C_3 controls t_5.

The supply must either have a source resistance of less than 2Ω at LF or be decoupled by at least $500\mu F$ so that it is not affected by the current surge resulting from a sudden input on pin 1.

In a receiver for both AM and SSB using an SL623C detector/carrier AGC generator, the AGC outputs of the SL621C and SL623C may be connected together provided that no audio reaches the SL621C input while the SL623C is controlling the system.

AGC lines may require some RF decoupling but the total capacitance on the output should not exceed 15000pF or the impulse suppression will suffer.

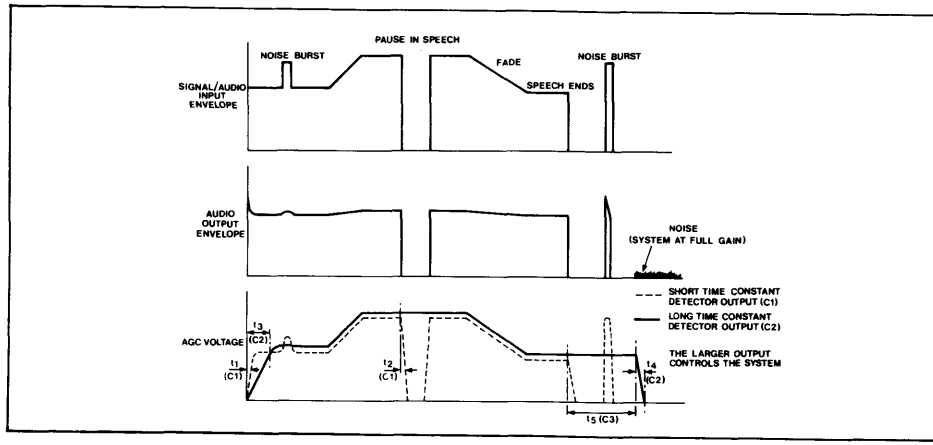

Fig. 3 Dynamic response of a system controlled by SL621C AGC generator

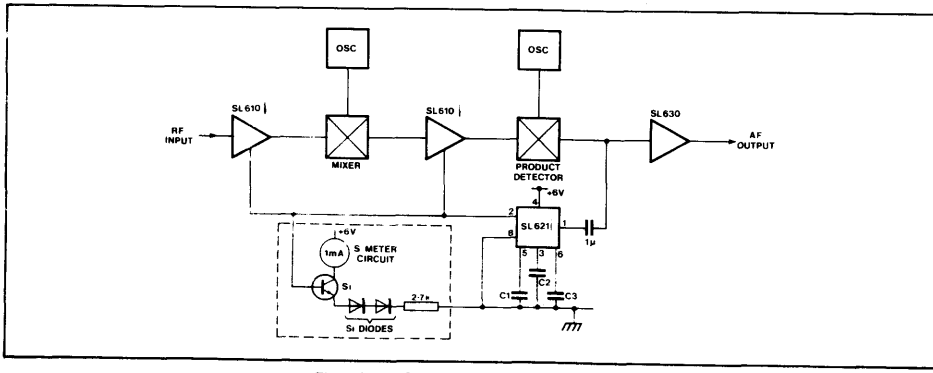

Fig. 4 SL621C used to control SSB receiver

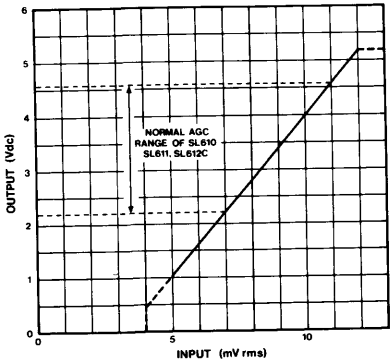

Fig. 5 Transfer characteristic of SL621C (typical)

Under some conditions,overload of the AGC output may occur in a receiver. Possible solutions are shown in Figs.6 and 7.

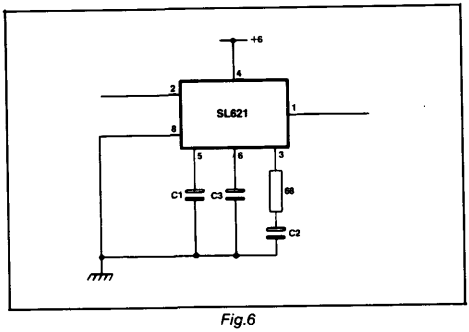

Fig.6

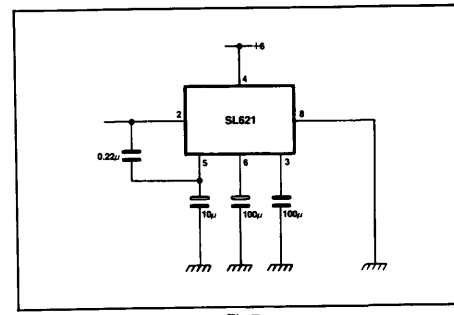

Fig.7

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SL623C

AM DETECTOR, AGC AMPLIFIER & SSB DEMODULATOR

The SL623C is a silicon integrated circuit combining the functions of low level, low distortion AM detector and AGC generator with SSB demodulator. It is designed specially for use in SSB/AM receivers in conjunction with SL610C, SL611C and SL612C RF and IF amplifiers. It is complementary to the SL621C SSB AGC generator.

The AGC voltage is generated directly from the detected carrier signal and is independent of the depth of modulation used. Its response is fast enough to follow the most rapidly fading signals. When used in a receiver comprising one SL610C and one SL612C amplifier, the SL623C will maintain the output within a 5dB range for a 90dB range of receiver input signal.

The AM detector, which will work with a carrier level down to 100mV, contributes negligible distortion up to 90% modulation. The SSB demodulator is of single balanced form. The SL623C is designed to operate at intermediate frequencies up to 30MHz. In addition it functions at frequencies up to 120MHz with some degradation in detection efficiencies.

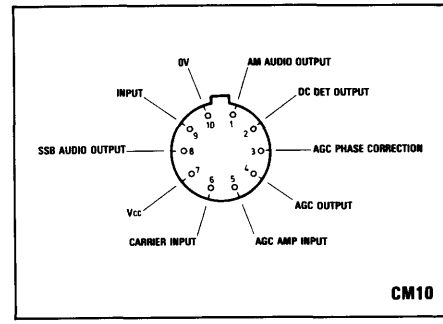


Fig. 1 Pin connections (bottom view)

FEATURES

- Negligible Distortion
- Easy Interfacing
- Fast Response Time

APPLICATIONS

- AM SSB Receivers
- Test Equipment

QUICK REFERENCE DATA

- Supply Voltage: 6V
- Maximum Frequency: 30MHz

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: −55°C to +125°C

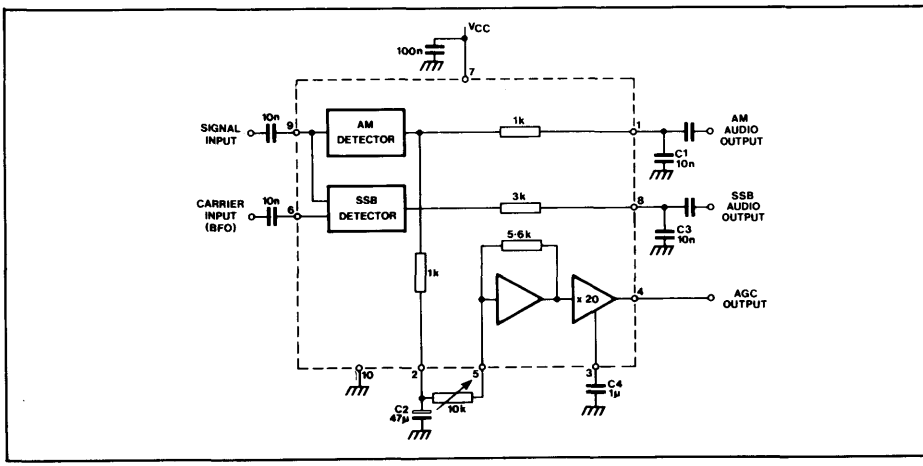


Fig. 2 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC} = 6V
Ambient temperature = −30°C to +85°C
Test circuit as Fig. 2

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		9	11	mA	No signal, Pin 4 open
Input impedance		800		Ω	Pins 6, 9
SSB audio output	22	30	47	mV rms	Signal input 20mV rms @ 1.748 MHz. Ref. signal input 100mV @ 1.750 MHz
AM audio output	43	55	67	mV rms	Signal input 125mV rms @ 1.75MHz modulated to 80% at 1kHz
AGC range (Note 1)			6	dB	Initial signal input 125mV rms at 1.75MHz modulated to 80% at 1kHz. Output set to 2.0V with 10kΩ potentiometer between Pins 2 & 5.

NOTES
1. The AGC range is the change in input level to increase AGC output voltage from 2.0V to 4.6V

APPLICATION NOTES

AGC Generator

Pin 3, the AGC amplifier phase correction point should be decoupled to ground by a 1 microfarad capacitor (C4), keeping leads as short as possible. The value of C4 is quite critical, and should not be altered: if it is increased the increased phase shift in the AGC loop may cause the receiver to become unstable at LF and if it is reduced the modulation level of the incoming signal will be reduced by fast-acting AGC.

The AGC output (Pin 4) will drive at least two SL610/11/12 amplifiers. The SL623AGC output is an emitter follower similar to that of the SL621C. Hence the outputs of the two devices may be connected in parallel when constructing AM/SSB systems.

Less signal is needed to drive the SSB demodulator than the AM detector. In a combined AM/SSB system, therefore, the signal will automatically produce an SSB AGC voltage via the SL621C as long as a carrier (BFO) is present at the input to the SSB demodulator of the SL623C. The AGC generator of the SL623 will not contribute in such a configuration.

For AM operation the BFO must be disconnected from the carrier input of the SSB demodulator. In the absence of an input signal, the SL621C will then return to its quiescent state. To switch over a receiver using the SL623C from SSB to AM operation it is therefore necessary to turn off the BFO and transfer the audio pick-off from the SSB to the AM detector.

Neglecting to disconnect the SSB carrier input during AM operation can result in heterodyning due to pick-up of carrier on the input signal. In some sets different filters are used for AM and SSB; these will also need to be switched.

The 10 kilohm gain-setting preset potentiometer is adjusted so that a DC output of 2 volts is achieved for an input of 125mV rms. There will then be full AGC output from the SL623C for a 4dB increase in input. A fixed resistor of 1.5 kilohms can often be used instead of the potentiometer.

SSB Demodulator

The carrier input is applied to Pin 6, via a low-leakage capacitor. It should have an amplitude of about 100mV rms and low second harmonic content to avoid disturbing the DC level at the detector output.

Pin 8 is the SSB output and should be decoupled at RF by a 0.01 microfarad capacitor. The output impedance of the detector is 3 kilohm and the terminal is at a potential of about +2V which may be used to bias an emitter follower if a lower output impedance is required. The input to the audio stage of a receiver using an SL623C should be switched between the AM and the SSB outputs — no attempt should be made to mix them. Since the SL621C is normally used in circumstances where low-level audio is obtained from the detector, the relatively high SSB audio output of the SL623C must be attenuated before being applied to the SL621C. This is most easily done by connecting the SL623C to the SL621C via a 2 kilohm resistor in series with a 0.5 microfarad capacitor.

Input Conditions

The input impedance is about 800 ohms in parallel with 5pF. Connection must be made to the input via a capacitor to preserve the DC bias. An input of about 125mV rms is required for satisfactory carrier AGC performance and 20mV rms for SSB detection. Normally, the AGC will cope with this variation but in an extreme case a receiver using an SL623C and having the same gain to the detector in both AM and SSB modes will be some 10dB less sensitive to AM.

PLESSEY
Semiconductors

SL640C & SL641C

DOUBLE BALANCED MODULATORS

The SL640C and SL641C are double balanced modulators intended for use in radio systems at frequencies up to 75MHz. The SL640 has an integral output load resistor (Pin 5) together with an emitter follower output (Pin 6) whereas the SL641 has a single output designed as a current drive to a tuned circuit.

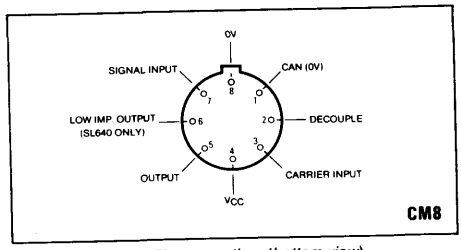


Fig. 1 Pin connections (bottom view)

FEATURES

- No External Bias Networks Needed
- Easy Interfacing
- Choice of Voltage or Current Outputs

APPLICATIONS

- Mixers In Radio Transceivers
- Phase Comparators
- Modulators

QUICK REFERENCE DATA

- Supply Voltage: 6V
- Conversion Gain: 0dB
- Maximum Inputs: 200mV rms

ABSOLUTE MAXIMUM RATINGS

Supply voltage 9V
Storage temperature: −55°C to +125°C

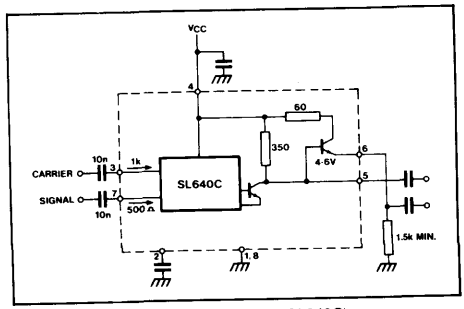


Fig. 2 Block diagram (SL640C)

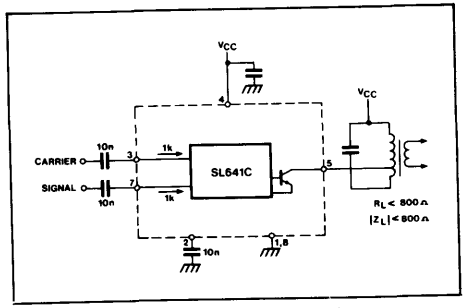


Fig. 3 Block diagram (SL641C)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC}: 6V
Ambient temperature: −30°C to +85°C

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	SL640C		12	17	mA	
	SL641C		10	13	mA	
Conversion gain	SL640C	−3	0	+3	dB	
Conversion transconductance	SL641C	1.75	2.5	3.5	mmho	
Noise figure			10		dB	
Carrier input impedance			1		kΩ	
Signal input impedance	SL640C		500		Ω	
	SL641C		1		kΩ	
Maximum input voltage	SL640C		210		mV rms	
	SL641C		250		mV rms	
Signal leak	SL640C		−30	−18	dB	Signal: 70mV rms, 1.75MHz Carrier: 100mV rms, 28.25 MHz Output: 30MHz
Carrier leak	SL640C		−30	−20	dB	
Signal leak	SL641C		−18	−12	dB	Signal: 70mV rms, 30MHz Carrier: 100mV rms, 28.25 MHz Output: 1.75MHz
Carrier leak	SL641C		−25	−12	dB	
Intermodulation products	SL640C		−45	−35	dB	Signal1: 42.5mV rms, 1.75MHz Signal2: 42.5mV rms, 2MHz Carrier: 100mV rms, 28.25MHz Output: 29.75MHz
	SL641C		−45	−30	dB	Signal1: 42.5mV rms, 30MHz Signal2: 42.5mV rms, 31MHz Carrier:100mV rms, 28.25MHz Output: 3.75MHz

APPLICATION NOTES

The SL640C and SL641C require input and output coupling capacitors which normally should be chosen to present a low reactance compared with the input and output impedances (see Electrical Characteristics). However, for minimum carrier leak at high frequencies the signal input should be driven from a low impedance source, in which case the signal input capacitor reactance should be comparable with the source impedance. Pin 2 must be decoupled to earth via a capacitor which presents the lowest possible impedance at both carrier and signal frequencies. The presence of these frequencies at Pin 2 would give rise to poor rejection figures and to distortion.

The output of the SL641C is an open collector. If both sidebands are developed across the load its dynamic impedance must be less than 800 ohms. If only one sideband is significant this may be raised to 1600 ohms and it may be further raised if the maximum input swing of 200mV rms is not used. The DC resistance of the load should not exceed 800 ohms. If the circuit is connected to a +6V supply and the load impedance to +9V, the load may be increased to 1.8 kilohms at AC or DC. This, of course increases the gain of the circuit.

There are two outputs from the SL640C; one is a voltage source of output impedance 350 ohms and 8pF and the other is the emitter of an emitter follower connected to the first output. The output on pin 6 requires a discrete load resistor of not less than 1500 ohms to ground. The emitter follower output should not be used to drive capacitive loads as emitter followers act as detectors under such circumstances with resultant distortion and harmonic generation. Frequency-shaping components may be connected to the voltage output and the shaped signal taken from the emitter follower. The AC load should not be less than 250 ohms.

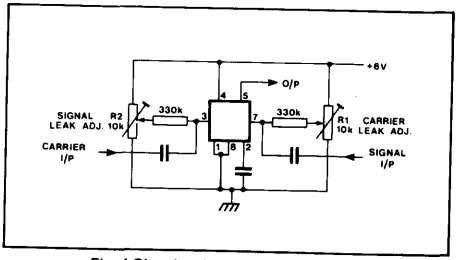


Fig. 4 Signal and carrier leak adjustment

Signal and carrier leak may be reduced by altering the bias on the carrier and signal input pins, as shown in Fig.4. With carrier but no signal R1 is adjusted for minimum carrier leak. A similar network is connected to the carrier input and with signal and carrier present, signal leak is minimised by means of R2.

PLESSEY
Semiconductors

SL650B & C SL651B & C

MODULATOR/PHASE LOCKED LOOP CIRCUITS FOR MODEMS

The SL650/1 are versatile integrated circuits capable of performing all the common modulation functions (AM, PAM, SCAM, FM, FSK, PSK, PWM, tone-burst, delta-modulation, etc.). A wide variety of phase-locked loops can be realised using the SL650 or SL651, with all parameters accurately controllable; they can also be used to generate precise waveforms at frequencies up to 0.2MHz.

The highly accurate and stable variable frequency oscillator is programmable over a wide range of frequency by voltage, current, resistor or capacitor. In addition direct selection of one of four spot frequencies is facilitated by using the on-chip binary interface, which accepts standard logic levels at very low logic '1' input currents.

The differential input phase comparator has a wide common mode input voltage range. It has a high gain limiting amplifier at its input requiring only 1mV input to maintain lock range in a typical phase-locked loop. The current output is programmable from zero to over 2mA by an external resistor or current input, and the gain is voltage –, current –, or resistance – programmable from zero to greater than 10,000.

An auxiliary amplifier with a voltage gain of, typically, 5000 is incorpated in the SL650 for use when it is required to interface to specified levels and impedances. The auxiliary amplifier features low bias current (typically 25nA), fast recovery from overload, and a short-circuit output current of ±7.5mA.

The auxiliary amplifier is omitted from the SL651.

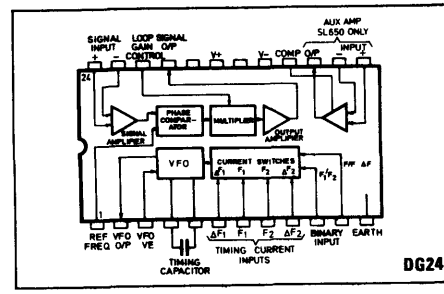


Fig.1 Pin connections (top view)

FEATURES

- VFO Frequency Variable Over 100:1 Range With Same Capacitor: Linearity 0.2%
- VFO Temperature Coefficient:
  'B' Types 20 ppm/°C Max.
  'C' Types 20 ppm/°C Typ.
- Supply sensitivity 20 ppm/% Typ.
- VFO Phase-Continuous at Transitions
- Binary Interface
- Phase Comparator O/P Can Swing to Supply Voltages
- On-Chip Auxiliary Amplifier (SL650)

APPLICATIONS

- Modems
- Modulators
- Demodulators
- Tone Decoders
- Tracking Filters
- Waveform Generators

QUICK REFERENCE DATA

- Supply Voltages ±6V
- Operating Temperature Range –55°C to +125°C

ELECTRICAL CHARACTERSTICS

Test conditions (unless otherwise stated)
Supply voltage ±6V
Temperature T_A +22°C ±2°C)

Characteristics	Pins	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current I_{CC}	17,19			3	mA	
Variable frequency oscillator						
Initial frequency offset error		−3	±1	+3	%	
Normal mark/space ratio		0.98	1.00	1.02	–	
Temp. coefficient of frequency			±20		ppm/°C	See note 1
Frequency variation with supplies	17, 19		±20		ppm/%	
Voltage at timing current inputs	6, 7, 8, 9		±10		mV	See note 2
VFO output, 'low' state	2		0	0.2	V	
VFO output, 'high' state	2	+1.1	+1.3		V	$R_L \geqslant 10k\Omega$
Max. freq. of oscillation			0.5		MHz	
Binary inputs						
V_{in} to guarantee logic 'low'	10. 11			+0.6	V	See note 3
V_{in} to guarantee logic 'high'	10, 11	+2.4			V	
Input current	10, 11		0.05	0.25	mA	V_{in} = +3.0V
Phase comparator						
Differential I/P offset voltage	23, 24		±2		mV	V_{out} = 0V
Input bias current	23, 24		0.05	2.5	μA	V_{in} = 0V
Differential input resistance	23, 24		100		kΩ	
Common mode I/P voltage range	23, 24	±4			V	
Differential I/P to limit (AC)	23, 24		1.0	10	mV rms	See note 4
Output current	21, 22	±1.0	±2.0	±5.0	mA	I_{22} = 250μA
Current gain (pin 22 to pin 21)	21, 22	±4	±10		–	See note 5
Transconductance, O/P/diff.I/P	21,23,24	±100	±250		mA/V	See note 5
Output voltage, linear range	21	±5	±5.5		V	
Output current	21			±2	μA	I_{22} = 0
Phase comparator I/P 'low'	1	−4		−0.2	V	
Phase comparator I/P 'high'	1	+1.9		+5.3	V	
Auxiliary amplifier (SL650 only)						
Differential I/P offset voltage	13, 14		±2		mV	V_{out} = 0V
Input bias current	13, 14		0.025	0.5	μA	V_{in} = 0V
Differential I/P resistance	13, 14	0.2	3		MΩ	
Common mode I/P voltage range	13, 14	±4			V	
Voltage gain (13–14) to 15	13,14,15	1000	5000		–	
Output voltage range	15	±4	±4.8		V	$R_L \geqslant 2k\Omega$
Output current limit	15	±4	±6.5	±12	mA	

NOTES

1. With a timing current of 60μA and f = 1kHz (C = 0.01μF, R = 100kΩ, supply voltages = ±6V), the temperature coefficient of frequency of the SL650C is typically ±2.5ppm/°C over the range 0°C to +40°C.
2. This voltage applies for timing currents in the range 20μA to 2mA and with the relevant input selected. In the unselected state the voltage is typically +0.6V.
3. The 'low' state is maintained when the inputs are open-circuited.
4. Limiting will occur earlier if the output (pin 21) voltage-limits first.
5. For a control current input to pin 22 of 250μA The sign of the transconductance is positive when the signal input is positive and the VFO output (or phase comparator input) is 'high'.

ABSOLUTE MAXIMUM RATINGS

Supply voltages	± 7.5V
Storage temperature	−55° to +175°C
Operating temperature	−55° to +125°C
Input voltages	Not greater than supplies

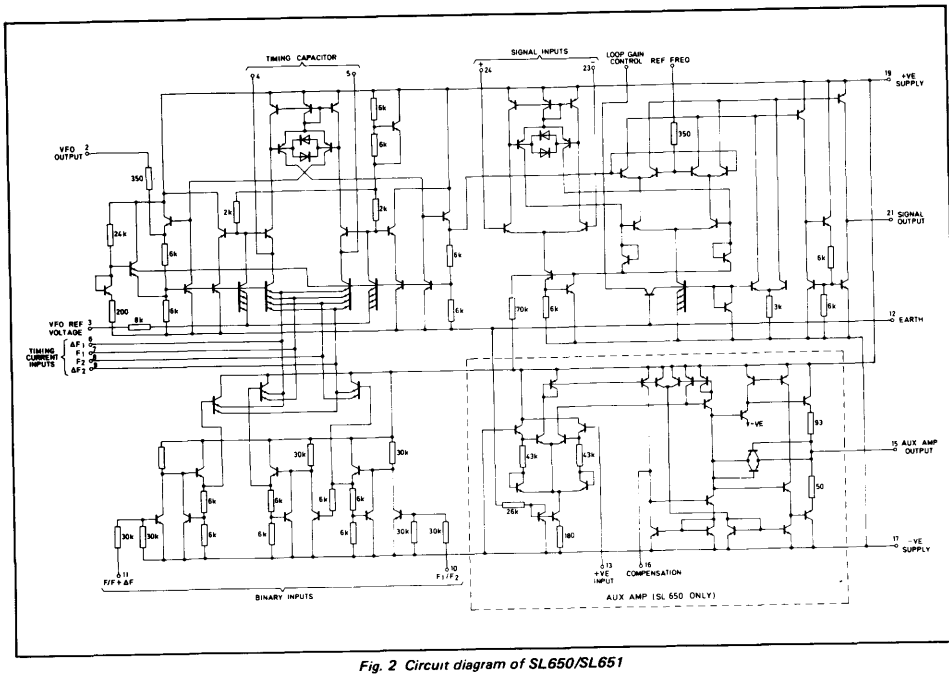


Fig. 2 Circuit diagram of SL650/SL651

OPERATING NOTES

Basic VFO Relationships

The VFO free-running frequency is inversely proportional to the value of the tuning capacitor C, connected to pins 4 and 5, and directly proportional to the VFO timing current (see Fig.3). Four current switches, controlled by TTL-compatible logic inputs on pins 10 and 11 select a combination of external resistors (connected to pins 6, 7, 8 and 9) which determine the VFO timing current. When both logic inputs are low, open-circuit, or connected to 0V however, then only the current switch associated with pin 7 is closed. the VFO timing current is then determined solely by the value of one resistor (R2 in Fig.3), and by the negative voltage connected to that resistor.

In this simplified configuration, as shown in Fig.4 the VFO frequency is determined by the relationship.

$$f = \frac{1}{CR} \cdot \frac{V_R}{V_3}$$

where f is in kHz, V in volts, C in μF and R in kΩ.

If the timing resistor R is returned to the VFO negative supply (pin 3), then

$$V_R = V_3$$

and $$f = \frac{1}{CR}$$

Pin 3 is normally connected to the chip negative supply; if, however, pin 3 is connected to a separate negative supply then the VFO can be voltage-controlled, and the VFO frequency will be:

$$f = \frac{1}{CR} \cdot \frac{V-}{V_C}$$

where V– is the chip and timing resistor negative supply and V_C is the control voltage connected to pin 3

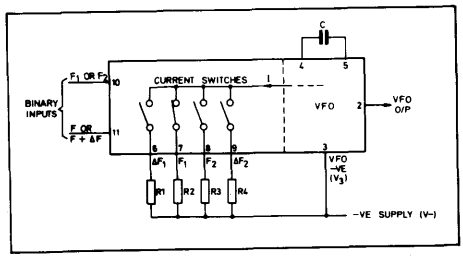


Fig. 3 VFO and binary interface

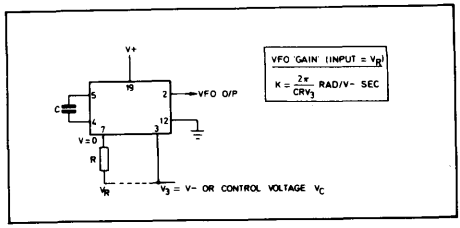


Fig. 4 VFO basic configuration

The timing current I should be between 20μA and 2mA, corresponding to a value for R between 3kΩ and 300kΩ with supplies of ±6V. For accurate timing, CR should be greater than 5μs.

When the binary interface is used as shown in Fig.3 the VFO free-running frequency is dependent on the logic input states, as shown in Table 1.

Pin 10	Pin 11	Timing Pins	VFO Frequency
LO	LO	7	$\frac{1}{CR_2}$
LO	HI	6 & 7	$\frac{1}{CR_2} + \frac{1}{CR_1}$
HI	LO	8	$\frac{1}{CR_3}$
HI	HI	8 & 9	$\frac{1}{CR_3} + \frac{1}{CR_4}$

Table 1 Binary interface relationships

Auxiliary amplifier

Internal compensation provides stability down to a closed loop gain of typically 20dB. A 30pF capacitor connected between pins 16 and 15 will give compensation down to a closed loop gain of unity. The output is short circuit protected but is not recommended for driving loads less than 2k

Phase Comparator

The phase comparator parameters are defined as follows (see Fig.5):

$$\text{Overall transconductance} = \frac{I_{21}}{V_{24} - V_{23}}$$

$$\text{Overall voltage gain} = \frac{V_{21}}{V_{24} - V_{23}}$$

The input amplifier will limit when the peak input ($V_{24} - V_{23}$) exceed ±5mV (typ.). It is recommended that R_L is kept below 5kΩ to avoid saturating the output and introducing de-saturation delays.

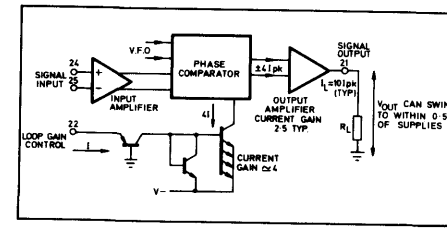


Fig. 5 Phase comparator

PLESSEY
Semiconductors

SL652C

MODULATOR/PHASE LOCKED LOOP

The SL652C is a versatile integrated circuit capable of performing all the common modulation functions (AM, PAM, SCAM, FM, FSK, PSK, PWM, tone-burst, delta-modulation, etc.). A wide variety of phase-locked loops can be realised using this device, with all parameters accurately controllable; they can also be used to generate precise waveforms at frequencies up to 0.2MHz.

The highly accurate and stable variable frequency oscillator is programmable over a wide range of frequency by voltage, current, resistor or capacitor. In addition direct selection of one of four spot frequencies is facilitated by using the on-chip binary interface, which accepts standard logic levels at very low logic '1' input currents.

The differential input phase comparator has a wide common mode input voltage range. It has a high gain limiting amplifier at its input requiring only 1mV input to maintain lock range in a typical phase-locked loop. The current output is programmable from zero to over 2mA by an external resistor or current input, and the gain is voltage – current – or resistance – programmable from zero to greater than 10,000.

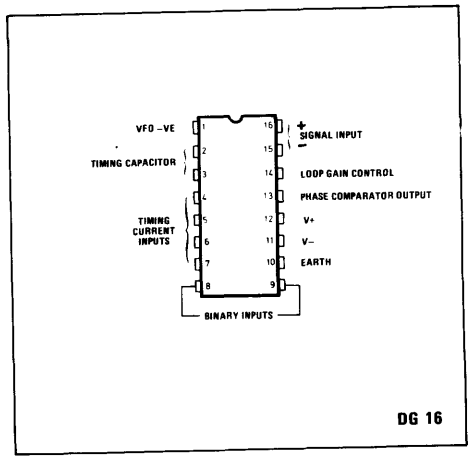


Fig. 1 Pin connections (top view)

FEATURES

- VFO Frequency Variable Over 100: 1 Range With Same Capacitor: Linearity 0.2%
- VFO Temperature Coefficient: 20 ppm/°C Typ.
- Supply sensitivity 20 ppm/% Typ.
- VFO Phase-Continuous at Transitions
- Binary Interface

APPLICATIONS

- Modems
- Modulators
- Demodulators
- Tone Decoders
- Tracking Filters
- Waveform Generators
- Stable Current-Controlled Oscillators

QUICK REFERENCE DATA

Supply Voltages	±6V
Operating Temperature Range	0°C to +70°C
Supply Currents	1.5mA typ.

ABSOLUTE MAXIMUM RATINGS

Supply voltages	±7.5V
Storage temperature	−55° to +175°C
Operating temperature	−55° to +125°C
Input voltages	Not greater than supplies

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Supply voltage: ±6V
T_A: +25°C ±5°C

Characteristics	Pins	Value			Units	Conditions
		Min.	Typ.	Max.		
Variable frequency oscillator						
Initial frequency offset error		−3	±1	+3	%	
Normal mark/space ratio		0.98	1.00	1.02	–	
Temp. coefficient of frequency			±20		ppm/°C	See note 1
Frequency variation with supplies	11, 12		±20		ppm/%	
Voltage at timing current inputs	4, 5, 6, 7		±10		mV	See note 2
Max. freq. of oscillation			0.5		MHz	
Binary inputs						
V_{in} to guarantee logic 'low'	8, 9			+0.6	V	See note 3
V_{in} to guarantee logic 'high'	8, 9	+2.4			V	
Input current	8, 9		0.05	0.25	mA	V_{in} = +3.0V
Phase comparator						
Differential I/P offset voltage	15, 16		±2		mV	V_{out} = 0V
Input bias current	15, 16		0.05	2.5	μA	V_{in} = 0V
Differential input resistance	15, 16		100		kΩ	
Common mode I/P voltage range	15, 16	± 4			V	
Differential I/P to limit (AC)	15, 16		1.0	10	mV	See note 4
Output current	13, 14	±1.0	±2.0	±5.0	mA	I_{14} = 250μA
Current gain (pin 14 to pin 13)	13, 14	±4	±10		–	See note 5
Transconductance, O/P/diff.I/P	13, 15, 16	±100	±250		mA/V	See note 5
Output voltage, linear range	13	±5	±5.5		V	
Output current	13			±2	mA	I_{14} = 0

NOTES

1. With a timing current of 60μA and f = 1kHz (C = 0.01μF, R = 100kΩ, supply voltages = ±6V), the temperature coefficient of frequency of the SL652C is typically ±2.5ppm/°C over the range 0°C to +40°C.
2. This voltage applies for timing currents in the range 20μA to 2mA and with the relevant input selected. In the unselected state the voltage is typically +0.6V.
3. The 'low' state is maintained when the inputs are open-circuited.
4. Limiting will occur earlier if the output (pin. 13) voltage-limits first.
5. For a control current input to pin. 14 of 250μA. The sign of the transconductance is positive when the signal input is positive and the VFO output (or phase comparator input) is 'high'.

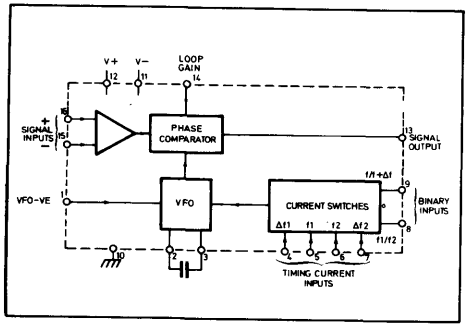


Fig. 2 SL652C block diagram

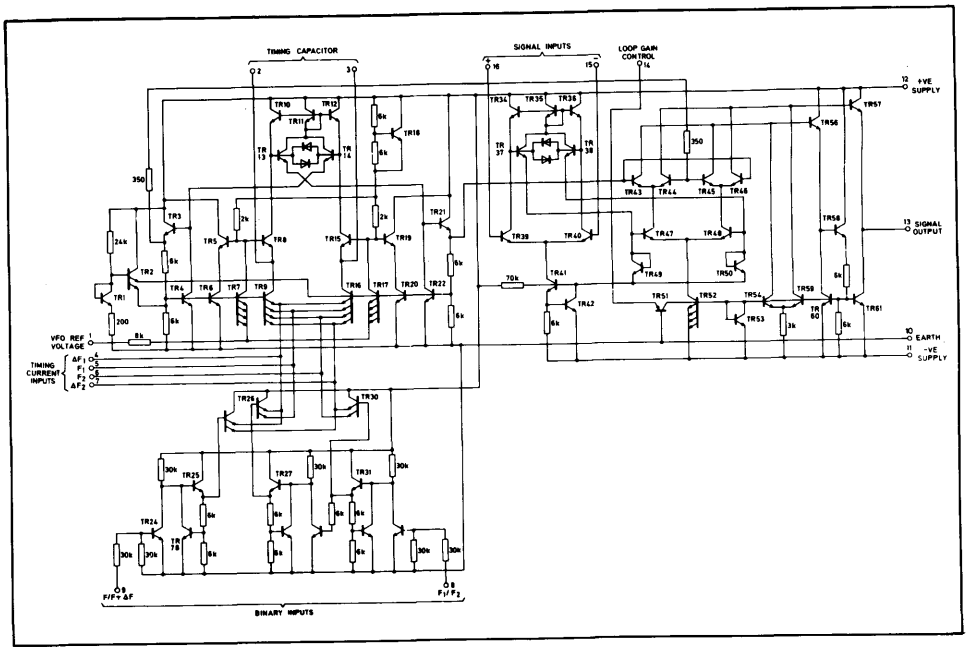


Fig. 3 Circuit diagram of SL652

OPERATING NOTES

Basic VFO Relationships

The oscillator output is normally taken from the phase comparator output by biasing the signal inputs a few hundred millivolts apart. If a direct oscillator output is required when the phase comparator is otherwise employed, it should be taken from pin 2 or 3 (which may affect oscillator stability). Alternatively, an SL651C can be used in place of the SL652C.

The VFO free-running frequency is inversely proportional to the value of the tuning capacitor C, connected to pins 2 and 3, and directly proportional to the VFO timing current (see Fig.4l). Four current switches, controlled by TTL-compatible logic inputs on pins 8 and 9 select a combination of external resistors (connected to pins 4, 5, 6 and 7) which determine the VFO timing current. When both logic inputs are low, open-circuit, or connected to OV however, then only the current switch associated with pin 5 is closed. The VFO timing current is then determined solely by the value of one resistor (R2 in Fig. 4), and by the negative voltage connected to that resistor.

In this simplified configuration, as shown in Fig. 5 the VFO frequency is determined by the relationship.

$$f = \frac{1}{CR}\frac{V_R}{V_1}$$

where f is in kHz, V in volts, C in μF and R in kΩ.

If the timing resistor R is returned to the VFO negative supply (pin 1) then

$$V_R = V_1$$

$$\text{and } f = \frac{1}{CR}$$

Pin 1 is normally connected to the chip negative supply; if, however, pin 1 is connected to a separate negative supply then the VFO can be voltage-controlled, and the VFO frequency will be:

$$f = \frac{1}{CR}\frac{V-}{V_C}$$

where V– is the chip and timing resistor negative supply and V_C is the control voltage connected to pin 1.

The timing current should be between 20μA and 2mA, corresponding to a value for R between 3kΩ and 300kΩ with supplies of ±6V. For accurate timing, CR should be greater than 5μs.

When the binary interface is used as shown in Fig. 4, the VFO free-running frequency is dependent on the logic input states, as shown in Table 1.

Pin 8	Pin 9	Timing Pins	VFO Frequency
LO	LO	5	$\frac{1}{CR_2}$
LO	HI	4 & 5	$\frac{1}{CR_2}+\frac{1}{CR_1}$
HI	LO	6	$\frac{1}{CR_3}$
HI	HI	6 & 7	$\frac{1}{CR_3}+\frac{1}{CR_4}$

Table 1 Binary interface relationships

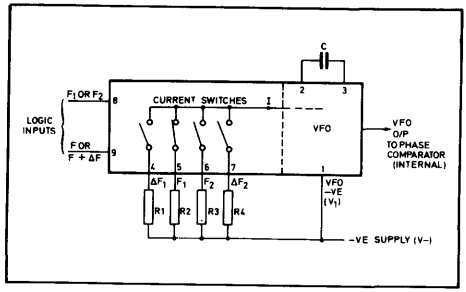


Fig. 4 VFO and binary interface

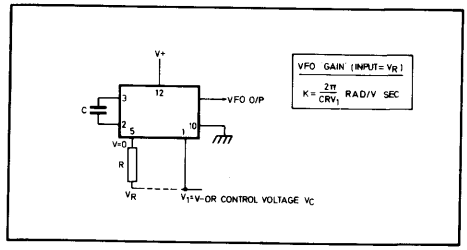


Fig. 5 VFO basic configuration

Phase Comparator

The phase comparator parameters are defined as follows (see Fig. 6):

$$\text{Overall transconductance} = \frac{I_{13}}{V_{16}-V_{15}}$$

$$\text{Overall voltage gain} = \frac{V_{13}}{V_{16}-V_{15}}$$

The input amplifier will limit when the peak input ($V_{16} - V_{15}$) exceeds ±5mV (typ.). It is recommended that R_L is kept below 5kΩ to avoid saturating the output and introducing de-saturation delays.

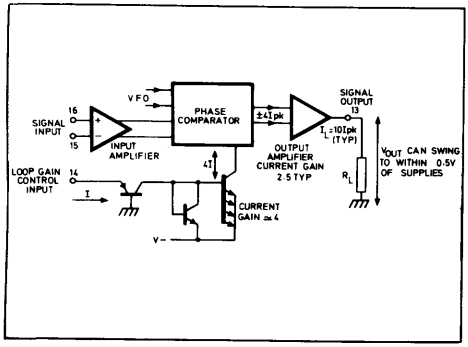


Fig 6. Phase comparator

PLESSEY
Semiconductors

SL1021 A & B

CHANNEL AMPLIFIER

The SL1021 A and B are bipolar monolithic integrated circuit amplifiers designed for use as channel amplifiers in telephone transmission equipment and satisfy the requirements of the British Post Office channel translating apparatus (RC5467).

The two variants A and B are distinguished by guaranteed output levels of +10dBm and +13dBm, respectively, other parameters being identical.

The main feature of these devices is the provision of a temperature-stable DC operated remote gain control facility having an adjustable range of control.

The connections provided allow a variety of uses, including fixed gain amplification with various feedback configurations.

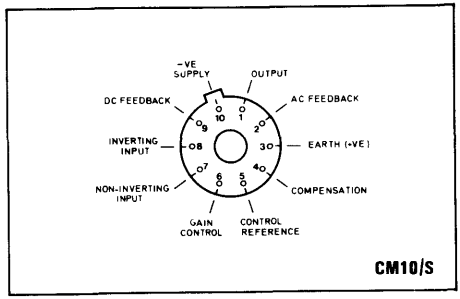


Fig. 1 Pin connections

FEATURES

- Up to +13dBm O/P into 600Ω (Class A)
- Temperature insensitive remote DC gain control
- Non-interactive adjustment of:
  - Gain
  - Gain Range
  - Output Return Loss
- 1:1 600Ω Transformer output can be optimized for low inductance using 2-element filter configuration
- Power Bandwidth: 150kHz (fixed gain, Fig. 4)
- Small Signal gain Bandwidth: 3MHz (see Fig. 4)

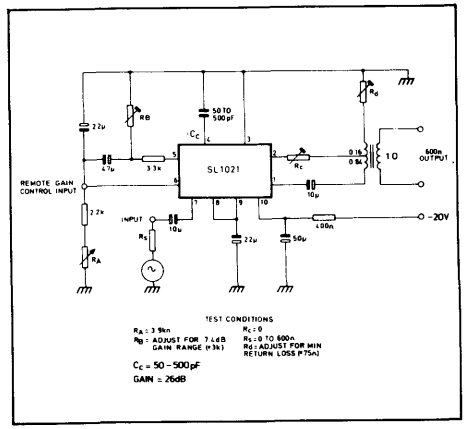


Fig. 2 SL1021 test circuit and typical application

APPLICATIONS

- Telephone Communications
- Channel Group Translation Equipment
- Radio – communications
- Small Signal Processing

QUICK REFERENCE DATA

Supply Voltage	−20V (via 400Ω)
Supply Current	9mA
Gain Control Current	0.5mA
Temperature Range	−25°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} 22°C ± 2°C
These characteristics are those obtained using the test circuit of Fig. 2, the gain range and output impedance being adjusted as indicated.

Characteristics	Value			Units	Conditions
	Min.	Typ,	Max.		
Gain (reference gain G)	24.5	26	27.5	dB	
Gain/R_S			28	dB	R_S = 600Ω to 3kΩ
Gain range		7.4		dB	Adjusted
Gain law					
R_A = 125Ω	3.9	4.1	4.3	dB	Relative to G
R_A = 9kΩ	−3.5	−3.3	−3.1	dB	
Gain/temperature	−0.1		+0.1	dB	Relative to G, T = 10°C to 45°C
Gain/V_S			0.1	dB	V_S = −20V ± 1V
Distortion					
2nd harmonic			−36	dBm0	At 10dBm output
3rd harmonic			−45	dBm0	
Overload					
SL1021A	10	13		dBm	Class A operation
SL1021B	13	15		dBm	
Noise			−76	dBmP	Proportional to G
Output impedance		600		Ω	Adjusted
Return loss	20			dB	250Hz to 3.4kHz
Input impedance	10			kΩ	Variable with R_A and R_S
Gain at reduced V_S	25.5			dB	V_S = −17.5V See Fig.2
Overload at reduced V_S	7			dBm	V_S = −17.5V
Gain control interaction between channels (change in gain for 3.3 mA current change)			0.25	dB	Equivalent to 11 channels, Common R_A earth return
Frequency response	240		3400	Hz	±0.05dB ref. 800Hz
Bandwidth			100	kHz	C_C = 50pF

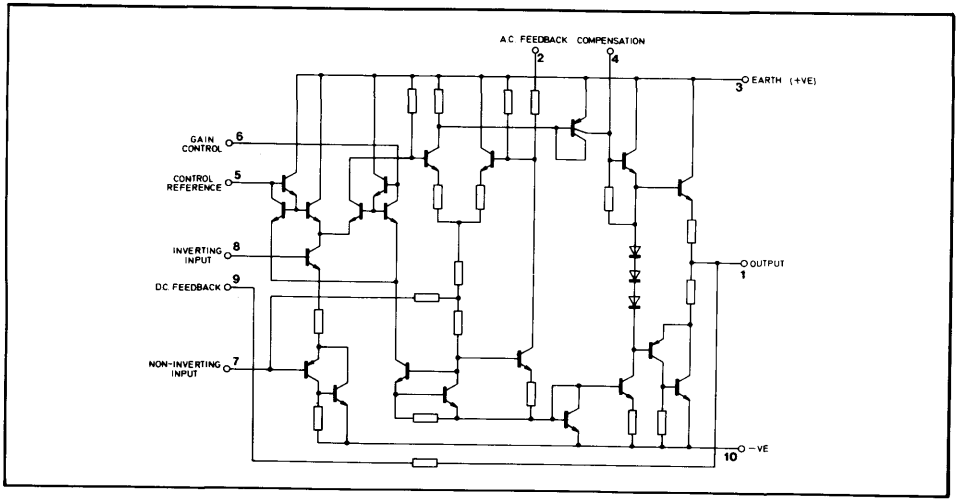


Fig. 3 SL1021 equivalent circuit

OPERATING CONDITIONS (see Fig. 2)

Parameter	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		9	11.0	mA	$R_A = 0$
		7.0		mA	$R_A = 11k\Omega$
Supply voltage		−20		V	Via 400Ω
Supply voltage on chip		−17		V	Pin 10
Supply maximum			−23	V	Pin 10
Control current		0.5		mA	$R_A = 0$
		0.26		mA	$R_A = 10k\Omega$
Control current change			0.3	mA	$R_A = 0$ to $11k\Omega$
Operational temp.	−25		+125	°C	
Fixed gain application (see Fig. 4)					
Optimum load		100		Ω	
Power output		20		mW	Class AB
Power bandwidth		150		kHz	10mW
Gain		20		dB	Values as Fig. 4
Frequency response		3		MHz	Small signal

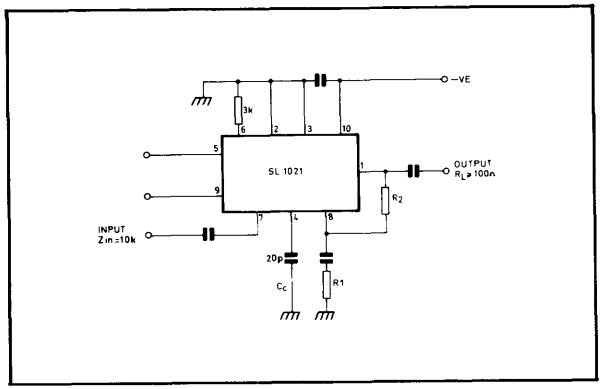


Fig. 4 Fixed gain amplifier, Class A or AB

OPERATING NOTES

1. The control decoupling capacitors should be of a low leakage type.
2. Other values of control resistors are possible if other gains/gain ranges are required. However, the parallel resistance to earth from pins 5 and 6 should be $\leqslant 8k\Omega$ at all settings.
3. If the control resistance is increased or open circuited, the amplifier gain will decrease to zero. (See Fig. 4 for fixed gain use).
4. The compensation capacitor can be increased to reduce the frequency response and power bandwidth.
5. The gain may be increased from the value of Fig. 2 (26dB nominal) by increasing R_c, the gain increase being given by:

$$\frac{R_c + 8.5}{8.5} \pm 20\%$$

where R_c is in $k\Omega$.

Because of temperature coefficient mismatch between R_C and internal resistors, the gain stability may be degraded with temperature.

6. The case is connected to pin 10 (–ve supply). To avoid damage to the device when operating with a positive earth system, care should be taken to prevent the case from becoming earthed.
7. This device is also available with tin-dipped leads, order as SL1021AM.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (via 400Ω)	–30V
Storage temp. range	–55°C to +175°C
Free air operating temp. range	–40°C to +130°C

PLESSEY
Semiconductors

SL1521A & C

300MHz WIDEBAND AMPLIFIERS

The SL1521A and C are wideband amplifiers intended for use in successive detection logarithmic IF strips operating at centre frequencies of up to 200MHz. It is a plug in replacement for the SL521 series of RF amplifiers. The mid-band voltage gain of the SL1521 is typically 12dB. The SL1521A and C differ mainly in the tolerance of voltage gain.

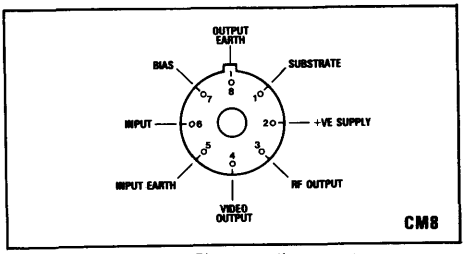


Fig.1 Pin connections

APPLICATIONS

- Radar IF Strips
- Wideband Amplification

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +150°C
Operating temperature	−55°C to +125°C
Maximum chip operating temperature	150°C
Chip to ambient thermal resistance	250°C/W

Test circuits: see Fig.8

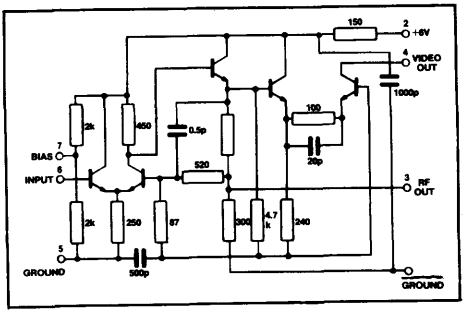


Fig.2 Circuit diagram

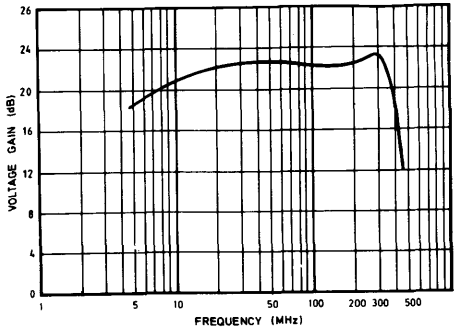


Fig.3 Voltage gain v. frequency

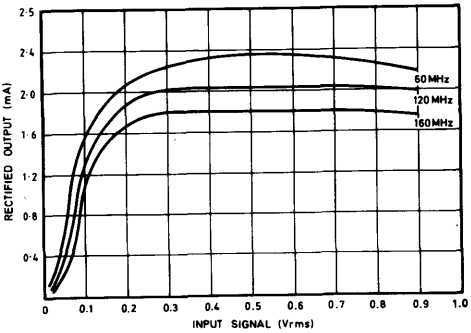


Fig.4 Rectified output current v. input signal

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Temperature = +22°C ±2°C
Supply voltage = +5.2V
DC connection between input and bias pins.

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Voltage gain, f = 120 MHz	SL1521 A	11.5		12.5	dB	
	SL1521 B	11.2		12.8	dB	3mVrms input
	SL1521 C	10.8		13.1	dB	50 ohms source
Voltage gain, f = 160MHz	SL1521 A	11.2		12.8	dB	8pF load + 500 Ω
	SL1521 B	11.0		13.0	dB	
	SL1521 C	10.6		13.4	dB	
Upper cut-off frequency	SL1521 A	315	350		MHz	
	SL1521 B	315	350		MHz	50 ohms source
	SL1521 C	300	350		MHz	
Lower cut-off frequency	All types		6	10	MHz	50 ohms source
Propagation delay	All types		0.6		ns	
Maximum rectified video output current	SL1521 A	0.95		1.05	mA	f = 120 MHz
	SL1521 B	0.90		1.10	mA	0.5Vrms input
	SL1521 C	0.90		1.20	mA	8pF load, 500 ohms in parallel
Variation of gain with supply voltage	All types		1.0		dB/V	
Variation of maximum rectified output current with supply voltage	All types		30		%/V	
Maximum input signal before overload	All types		1.5		V rms	See note below
Noise figure			3	4.5	dB	f = 120 MHz, source
Supply current	All types	10.0	15.0	20.0	mA	resistance optimised
Maximum RF output voltage	All types	1.0,			Vp-p	f=120MHz

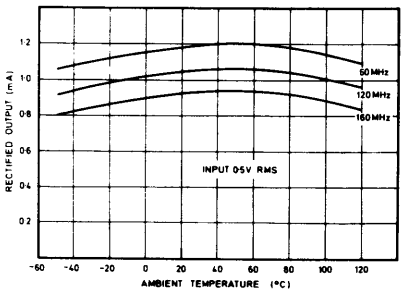


Fig. 5 Maximum rectified output current v. temperature

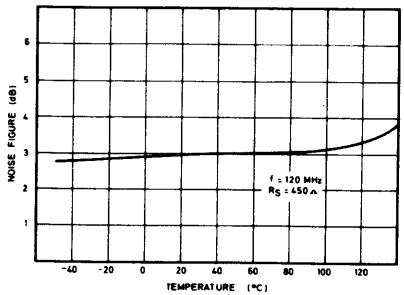


Fig. 6 Typical noise figure v. temperature

Operating Notes

The amplifiers are intended for use directly coupled, as shown in Fig. 8.

The seventh stage in an untuned cascade will be giving virtually full output on noise.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The choice of network is also controlled by the need to avoid distorting the logarithmic law; the network must give unity voltage transfer at resonance. A suitable network is shown in Fig. 9. The value of C1 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit.

A simple capacitor may not be suitable for decoupling the output line if many stages and fast rise times are required.

Values of positive supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in high frequency tuned cascades.

The amplifiers have been provided with two earth leads to avoid the introduction of common earth lead inductance between input and output circuits. The equipment designer should take care to avoid the subsequent introduction of such inductance.

	Number of stages			
	6 or more	5	4	3
Minimum capacitance	30nF	10nF	3nF	1nF

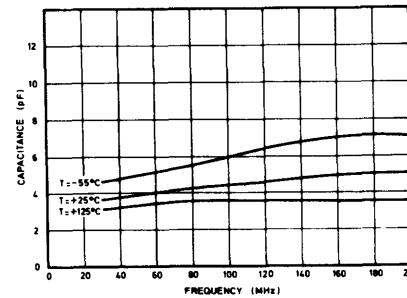


Fig. 7 Input admittance with open-circuit output

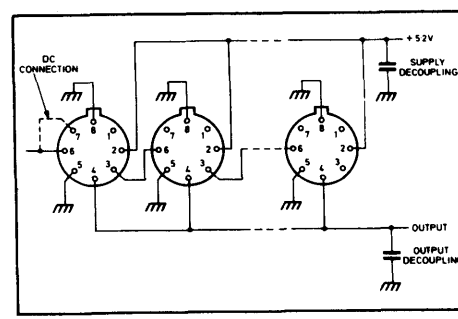


Fig. 8 Direct coupled amplifiers

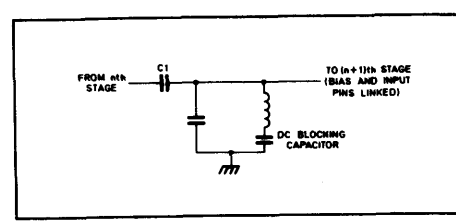


Fig. 9 Suitable interstage tuned circuit

PLESSEY
Semiconductors

SL1523C

DUAL WIDEBAND LOGARITHMIC AMPLIFIER

The SL1523C consists of two SL1521's in series, and is intended to reduce the package count and improve the packing density in logarithmic strips at frequencies up to 200 MHz.

Absolute Maximum Ratings (Non-Simultaneous)

The absolute maximum ratings are limiting values above which operating life may be shortened or satisfactory performance may be impaired.

Storage temperature range	−55°C to +175°C
Operating temperature	−55°C to +125°C
Chip operating temperature:	150°C
Chip-to-ambient thermal resistance	300°C/W
Chip-to-case thermal resistance	95° C/W
Maximum instantaneous voltage at video output	+12V
Supply voltage	+ 9V

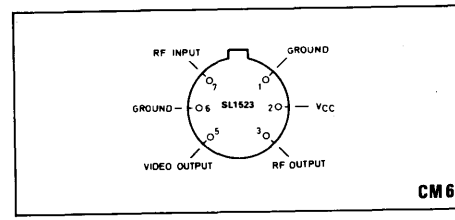


Fig. 1 Pin connections (bottom view)

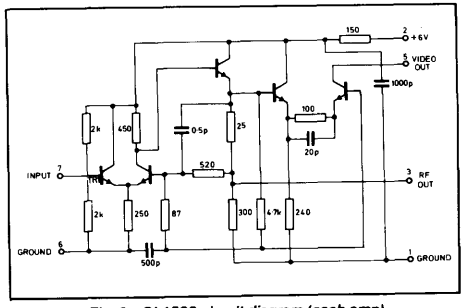


Fig. 2 SL1523 circuit diagram (each amp)

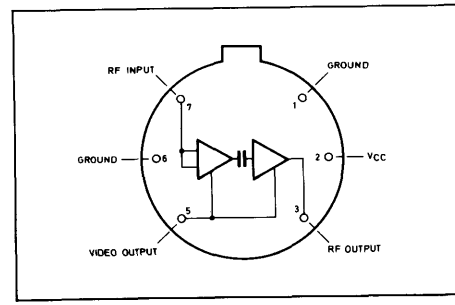


Fig. 3 SL1523 block diagram

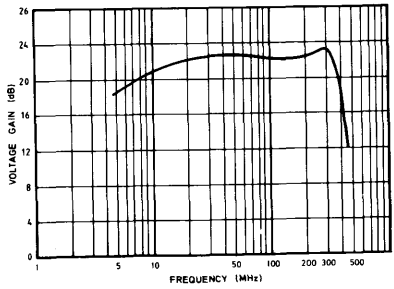


Fig. 4 Voltage gain v. frequency

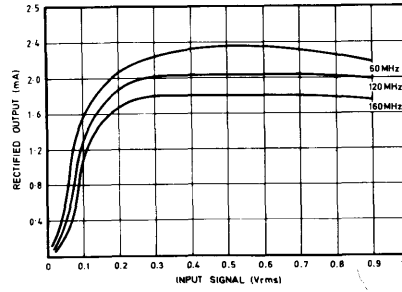


Fig. 5 Rectified output current v. input signal

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Temperature = 22°C ± 2°C
Supply voltage = + 5.2V

Characteristic		SL1523	Units	Test Conditions
Voltage gain	(Min)	21	dB	f = 120 MHz, 3 mV rms input, 50 ohms source 4 pF load + 500 ohms
	(Max)	27	dB	
Voltage gain	(Min)	20	dB	f = 160 MHz, 3 mV rms input, 50 ohms source 4 pF load + 500 ohms
	(Max)	27	dB	
Upper cut-off frequency	(Min)	300	MHz	50 ohms source
	(Typ)	325	MHz	50 ohms source
Lower cut-off frequency	(Typ)	8	MHz	50 ohms source
	(max)	10	MHz	50 ohms source
Propagation delay	(Typ)	1.2	ns	
Maximum rectified video output current	(Min)	1.6	mA	f=120 MHz, 0.5 V rms input, 4 pF load.
	(Max)	2.0	mA	
Variation of gain with supply voltage	(Typ)	2.0	dB/V	
Variation of maximum rectified output current with supply voltage	(Typ)	30	%/V	
Maximum input signal before overload	(Typ)	1.5	V rms	*See note below
Noise figure	(Typ)	3	dB	f=120 MHz, source resistance optimized
Supply current	(Min)	20	mA	
	(Typ)	30	mA	
	(Max)	40	mA	
Maximum R.F. output voltage	(Min)	1.0	Vp-p	f=120MHz

Note: Overload occurs when the input signal reaches a level sufficient to forward bias the base-collector junction of TR1 on peaks.

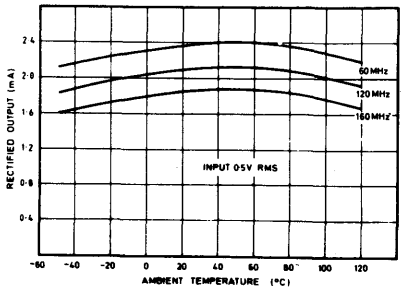


Fig. 6 Maximum rectified output current v. temperature

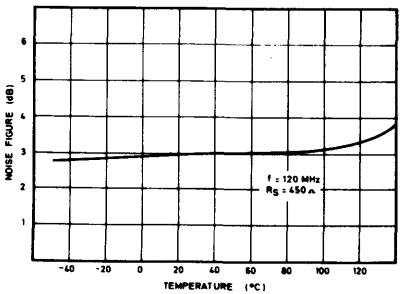


Fig. 7 Typical noise figure v. temperature

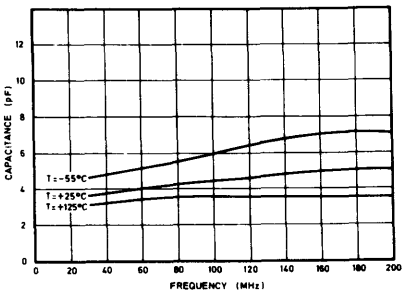


Fig. 8 Input admittance with open circuit output

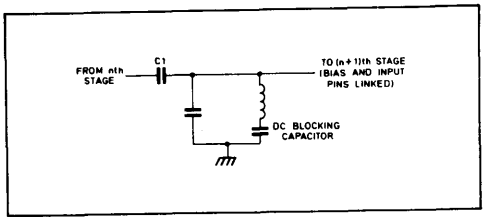


Fig. 9 Suitable interstage tuned circuit

PLESSEY
Semiconductors

SL1613C

WIDEBAND LOG IF STRIP AMPLIFIER

The SL1613C is a bipolar monolithic integrated circuit wideband amplifier intended primarily for use in successive detection logarithmic IF strips, operating at centre frequencies between 10MHz and 60MHz. The devices provide amplification, limiting and rectification, are suitable for direct coupling and incorporate supply line decoupling. The mid-band voltage gain of the SL1613C is typically 12dB.

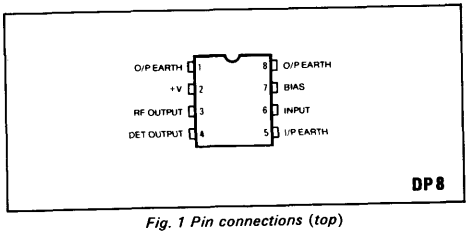


Fig. 1 Pin connections (top)

FEATURES

- Well Defined Gain
- 4.5dB Noise Figure
- High I/P Impedance
- Low O/P Impedance
- 150MHz Bandwidth
- On-Chip Supply Decoupling
- Low External Component Count

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	−55°C to +125°C
Operating temperature range	−30°C to +85°C
Maximum instantaneous voltage at video output	+12V
Supply voltage	9V

APPLICATIONS

- Logarithmic IF Strips with Gains up to 108dB and Linearity Better than 2dB

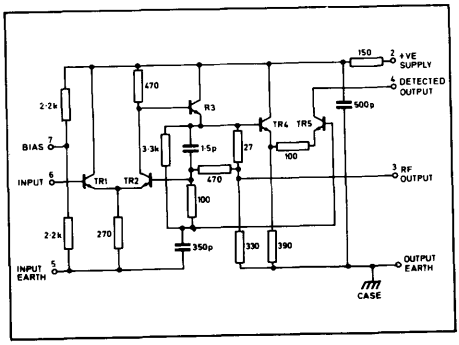


Fig. 2 Circuit diagram

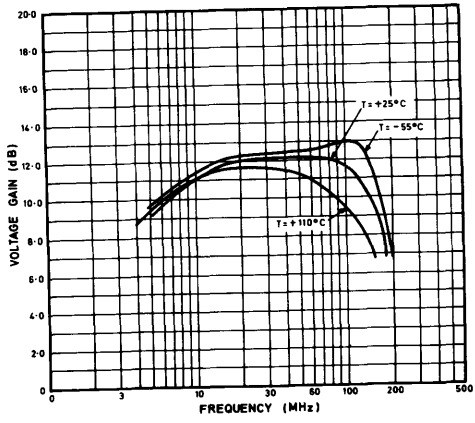


Fig. 3 Voltage gain v. frequency

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_A = +22°C ±2°C
Supply voltage = +6V
DC connection between input and bias pins

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	10	12	14	dB	f=30MHz, R_s=10Ω, C_L=8pF
Upper cut-off frequency (Fig. 3)		150		MHz	R_S=10Ω, C_L=8pF
Lower cut-off frequency (Fig. 3)		5		MHz	R_S=10Ω, C_L=8pF
Propagation delay		2		ns	
Max. rectified video output current (Figs. 4 and 5)	0.8	1	1.3	mA	f=60MHz, V_{in}=500mV rms
Variation of gain with supply voltage		0.7		dB/V	
Variation of maximum rectified output current with supply voltage		25		%V	
Maximum input signal before overload		1.9		V rms	See Note 1
Noise figure (Fig. 6)		4.5		dB	f=60MHz, R_s=450Ω
Maximum RF output voltage		1.2		Vp-p	
Supply current		15	20	mA	

Note 1. Overload occurs when the input signal reaches a level sufficient to forward bias the base collector junction of TR1 on peak.

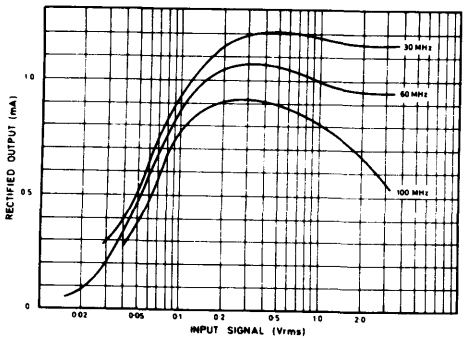


Fig. 4 Rectified output current v. input signal

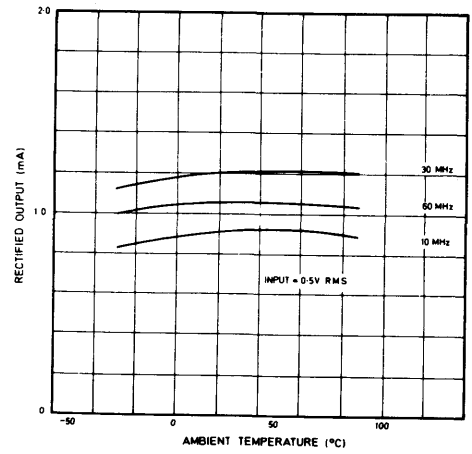


Fig. 5 Maximum rectified output current v. temperature

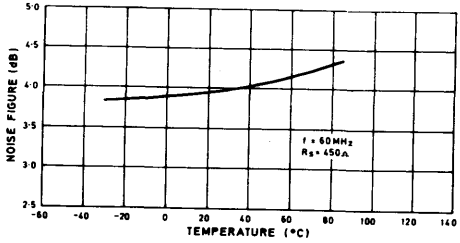


Fig. 6 Typical noise figure v. temperature

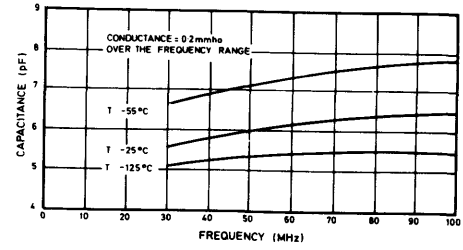


Fig. 7 Input admittance with open circuit output

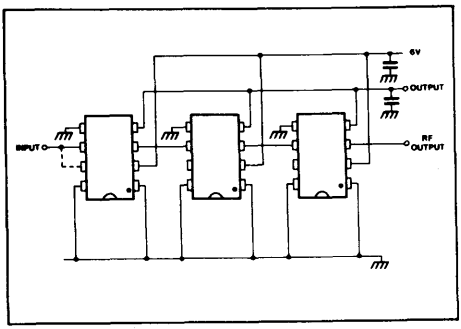


Fig. 8 Direct coupled amplifiers

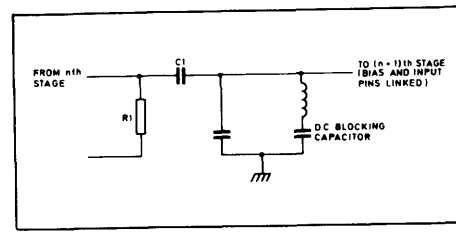


Fig. 9 Suitable interstage tuned circuit

OPERATING NOTES

The amplifiers are intended for use directly coupled, as shown in Fig. 8.

The seventh stage in an untuned cascade will be giving virtually full output on noise.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The choice of network is also controlled by the need to avoid distorting the logarithmic law; the network must give unity voltage transfer at resonance. A suitable network is shown in Fig. 9. The value of C1 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit. Resistor R1 may be introduced to improve the symmetry of filter response, providing other values are adjusted for unity gain at resonance.

A simple capacitor may not be suitable for decoupling the output line if many stages and fast rise times are required.

Values of positive supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in high frequency tuned cascades.

The amplifiers have been provided with two earth leads to avoid the introduction of common earth lead inductance between input and output circuits. The equipment designer should take care to avoid the subsequent introduction of such inductance.

	Number of stages			
	6 or more	5	4	3
Minimum capacitance	30nf	10nF	3nF	1nF

The 500pF supply decoupling capacitor has a resistance of, typically, 10Ω. It is a junction type having a low breakdown voltage and consequently the positive supply current will increase rapidly if the supply voltage exceeds 7.5V (See Absolute Maximum Ratings).

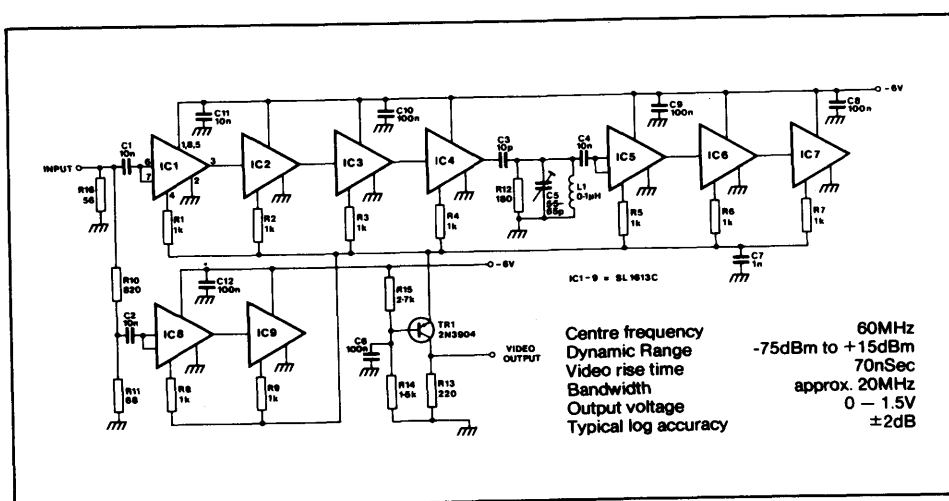


Fig. 10 Circuit diagram of low cost strip

PLESSEY
Semiconductors

SL1621C

AGC GENERATOR

The SL1621C is an AGC generator designed specifically for use in SSB receivers in conjunction with the SL1610C, SL1611C and SL1612CRF and IF amplifiers. In common with other advanced systems it generates a suitable AGC voltage directly from the detected audio waveform, provides a 'hold' period to maintain the AGC level during pauses in speech, and is immune to noise interference. In addition it will smoothly follow the fading signals characteristic of HF communication.

When used in a receiver comprising one SL1610C and one SL1612C amplifier and a suitable detector, the SL1621C will maintain the output within a 4dB range for a 110dB range of receiver input signal.

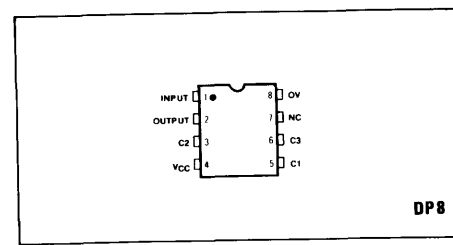


Fig. 1 Pin connections (top view)

FEATURES

- All Time Constants Set Externally
- Easy Interfacing
- Compatible with SL1610/1611/ 1612

APPLICATIONS

- SSB Receivers
- Test Equipment

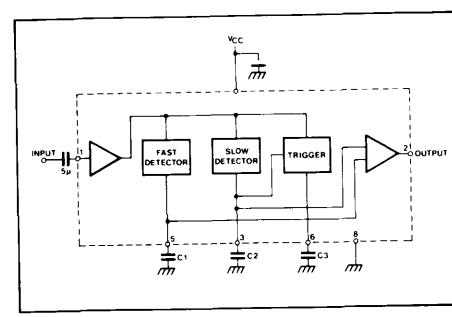


Fig. 2 Block diagram

QUICK REFERENCE DATA

- Supply voltage: 6V
- Supply current: 3mA

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC} = 6V
Ambient temperature: −30°C to +85°C
Test frequency: 1kHz
Test circuit as Fig. 2

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: −55°C to +125°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.1	5	mA	No signal
Cut-off frequency (−3dB)		6		kHz	
Input for 2.2V DC output		7		mVrms	
Input for 4.6V DC output		11		mVrms	
Maximum output voltage	4.5			V	
AC ripple on output		12		mV pk-pk	1kHz, output open circuit
Input resistance		500		Ω	
Output resistance		70		Ω	
'Fast' rise time t_1		20		ms	0 to 50% full output
'Fast' decay time t_2		200		ms	100% to 36% full output
'Slow' rise time t_3		200		ms	Time to output transistion point
Hold collapse time t_4		100		ms	90% to 10% full output
Hold time t_5		1.0		s	

APPLICATION NOTES

The SL1621C consists of an input AF amplifier coupled to a DC output amplifier by means of two detectors having short and long rise and fall times respectively. The time constants of these detectors are set externally by capacitors on pins 5 (C_1) and 3 (C_2).

The detected audio signal at the input will rapidly establish an AGC level via the 'fast' detector time in t_1 (see Fig. 3). Meanwhile the long time constant detector output will rise and after t_3 will control the output because this detector is more sensitive.

Input signals greater than approximately 4mV rms will actuate a trigger circuit whose output pulses provide a discharge current for C_2.

By this means the voltage on C_2 can decay at a maximum rate, which corresponds to a rise in receiver gain of 20dB/s. Therefore the AGC system will smoothly follow signals which are fading at this rate or slower. However should the receiver input signals fade faster than this, or disappear completely as during pauses in speech, then the input to the AGC generator will drop below the 4mV rms threshold and the trigger will cease to operate. As C_2 then has no discharge path, it will hold its charge (and hence the output AGC level) at the last attained value. The output of the short time constant detector will drop to zero in time t_2 after the disappearance of the signal.

The trigger pulses also charge C_3. When the trigger pulses cease, C_3 discharges and after t_5 C_2 is discharged rapidly (in time t_4) and so full receiver gain is restored. The hold time, t_5 is approximately one second with $C_3 = 100\mu F$. If signals reappear during t_5, then C_3 will recharge and normal operation will continue. The C_3 recharge time is made long enough to prevent prolongation of the hold time by noise pulses.

Fig. 3 shows how a noise burst superimposed on speech will initiate rapid AGC action via the short time constant detector while the long time constant detector effectively remembers the pre-noise AGC level.

The various time constants quoted are for $C_1 = 50\mu F$ and $C_2 = C_3 = 100\mu F$. These time constants may be altered by varying the appropriate capacitors. C_1 controls t_1, t_2; C_2 controls t_3, t_4; C_3 controls t_5.

The supply must either have a source resistance of less than 2Ω at LF or be decoupled by at least $500\mu F$ so that it is not affected by the current surge resulting from a sudden input on pin 1.

In a receiver for both AM and SSB using an SL1623C detector/carrier AGC generator, the AGC outputs of the SL1621C and SL1623C may be connected together provided that no audio reaches the SL1621C input while the SL1623C is controlling the system.

AGC lines may require some RF decoupling but the total capacitance on the output should not exceed 15000pF or the impulse suppression will suffer.

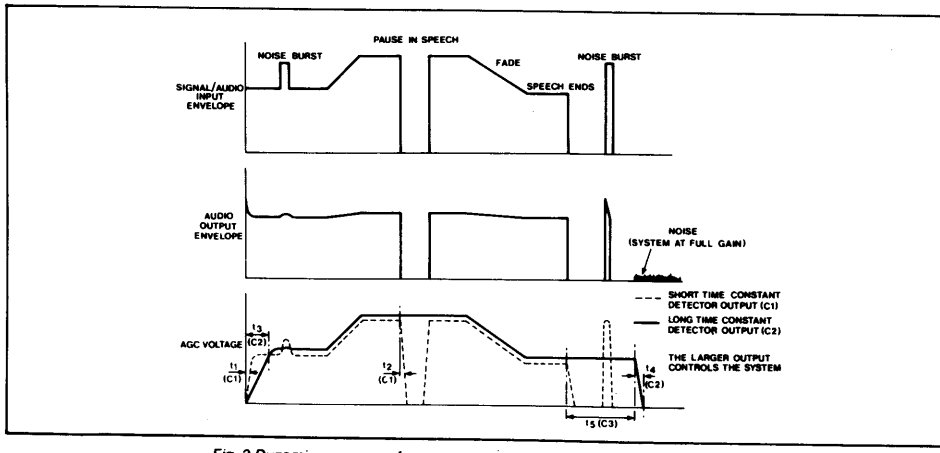


Fig. 3 Dynamic response of a system controlled by SL1621C AGC generator

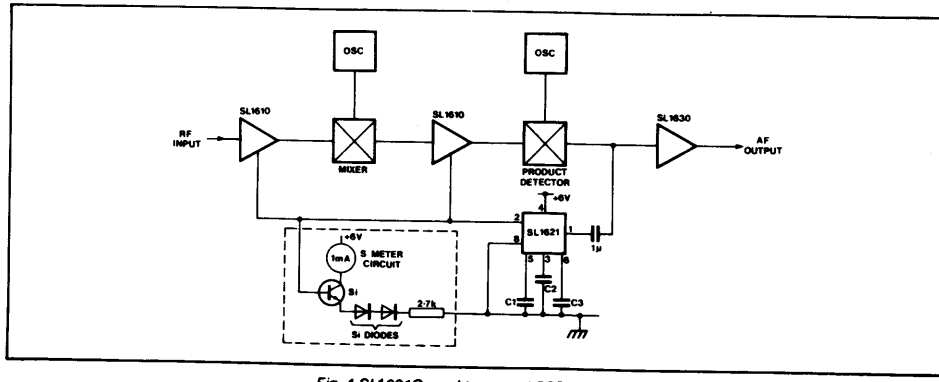


Fig. 4 SL1621C used to control SSB receiver

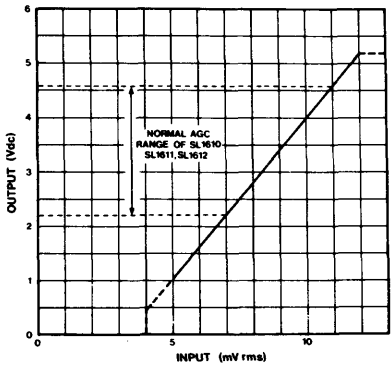


Fig. 5 Transfer characteristic of SL1621C (typical)

Under some conditions, overload of the AGC output may occur in a receiver. Possible solutions are shown in Figs.6 and 7.

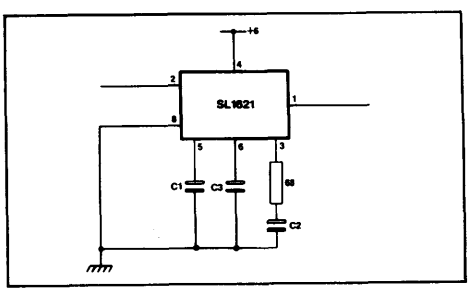


Fig.6

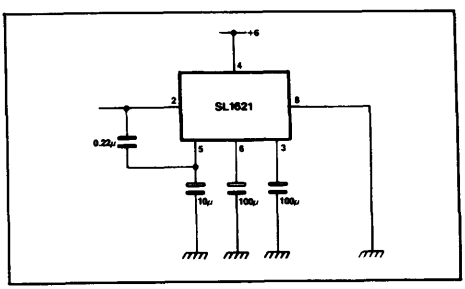


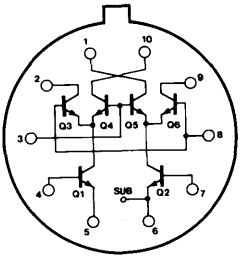
Fig.7

PLESSEY
Semiconductors

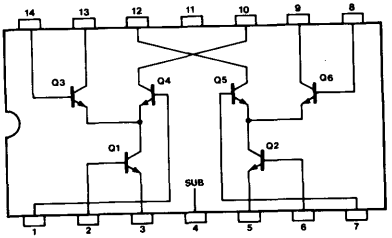
SL2363C & SL2364C

VERY HIGH PERFORMANCE TRANSISTOR ARRAYS

The SL2363C and SL2364C are arrays of transistors internally connected to form a dual long-tailed pair with tail transistors. They are monolithic integrated circuits manufactured on a very high speed bipolar process which has a minimum useable f_T of 2.5 GHz, (typically 5GHz).
The SL2363 is in a 10 lead TO5 encapsulation.
The SL2364 is in a 14 lead DIL plastic encapsulation.



SL2363C CM10



SL2364C DP14

Fig. 1 Pin connections (top view)

FEATURES

- Complete Dual Long-Tailed Pair in One Package.
- Very High f_T – Typically 5 GHz
- Very Good Matching Including Thermal Matching

APPLICATIONS

- Wide Band Amplification Stages
- 140 and 560 MBit PCM Systems
- Fibre Optic Systems
- High Performance Instrumentation
- Radio and Satellite Communications

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 22°C ±2°C

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
BV_{CBO}	10	20		V	I_C = 10µA
LV_{CEO}	6	9		V	I_C = 5mA
BV_{EBO}	2.5	5.0		V	I_E = 10µA
BV_{CIO}	16	40		V	I_C = 10µA
h_{FE}	20	80			I_C = 8mA, V_{CE} = 2V
f_T	2.5	5		GHz	I_C (Tail) = 8mA, V_{CE} = 2V
ΔV_{BE} (See note 1)		2	5	mV	I_C (Tail) = 8 mA, V_{CE} = 2V
$\Delta V_{BE}/T_{AMB}$		-1.7		mV/°C	I_C (Tail) = 8 mA, V_{CE} = 2V
C_{CB}		0.5	0.8	pF	V_{CB} = 0
C_{CI}		1.0	1.5	pF	V_{CI} = 0

NOTE 1. ΔV_{BE} applies to $|V_{BEQ3} - V_{BEQ4}|$ and $|V_{BEQ5} - V_{BEQ6}|$

TYPICAL CHARACTERISTICS

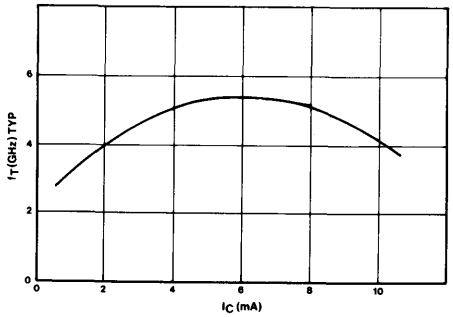


Fig. 2 Collector current

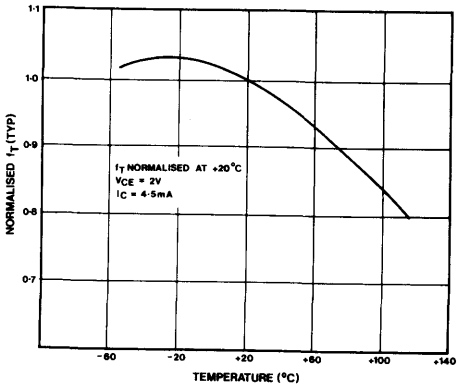


Fig. 3 Chip temperature

ABSOLUTE MAXIMUM RATINGS

Maximum individual transistor dissipation 200mW

Storage temperature	−55°C to +150°C
Maximum junction temperature	+150°C
Package thermal resistance (°C/W):	
Chip to case	65 (CM10)
Chip to ambient	225 (CM10) 175 (DP14)

V_{CBO} = 10V, V_{EBO} = 2.5V, V_{CEO} = 6V, V_{CIO} = 15V, IC (any one transistor) = 20mA

The substrate should be connected to the most negative point of the circuit to maintain electrical isolation between the transistors.

PLESSEY
Semiconductors

SL3045C SL3046C

GENERAL PURPOSE NPN TRANSISTOR ARRAY

The SL3045C and SL3046C are monolithic arrays of five general purpose transistors arranged as a differential pair and three isolated transistors. The arrays are available in ceramic (SL3045C) or plastic (SL3046C) 14 lead DIL packages.

FEATURES

- 5 General Purpose Monolithic Transistors
- Good Thermal Tracking
- Wide Operating Current Range
- Suitable for Operation from DC to VHF
- Low Noise Performance 3.5dB at 1kHz.

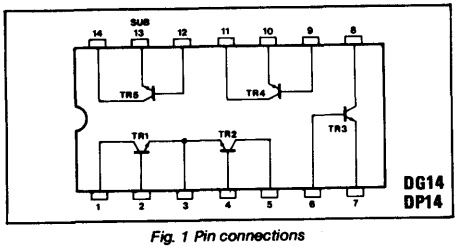


Fig. 1 Pin connections

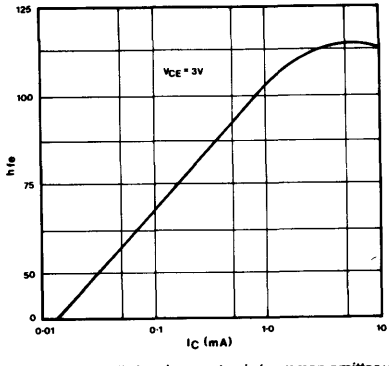


Fig. 2 Typical small signal current gain (common emitter vs. collector current)

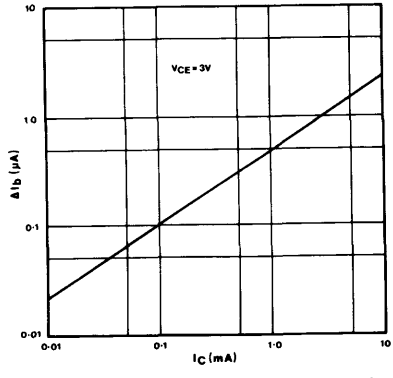


Fig. 3 Base current matching vs. collector current

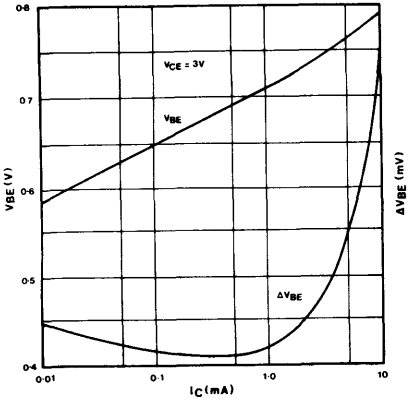


Fig. 4 Typical base emitter voltage and base emitter volt matching vs. collector current

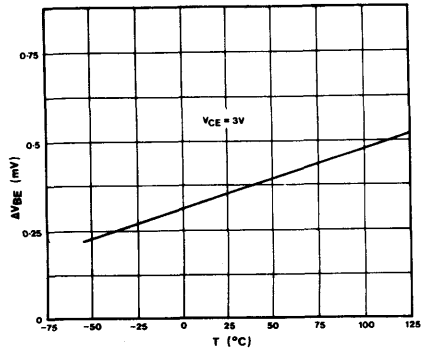


Fig. 5 Typical base emitter volt matching vs. chip temperature

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = 22°C \pm 2°C$

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Static characteristics						
Emitter base leakage	I_{EBO}		0.1	1	μA	$V_{EB} = 6V$
Collector emitter breakdown	LV_{CEO}	15	20		V	$I_C = 1mA$
Collector-base breakdown	BV_{CBO}	20	50		V	$I_C = 10\mu A$
Collector-subtrate breakdown	BV_{CIO}	20	70		V	$I_C = 10\mu A$
Collector cut off current	I_{CEO}			0.5	μA	$V_{CE} = 10V$, $I_B = 0$
	I_{CBO}			40	nA	$V_{CB} = 10V$, $I_B = 0$
Base emitter voltage	$V_{BE(ON)}$		0.71		V	$V_{CE} = 3V$, $I_C = 1mA$
Collector-emitter saturation	$V_{CE(SAT)}$		0.23		V	$I_B = 1mA$, $I_C = 10mA$
Static forward current-transistor ratio	H_{FE}		120			$V_{CE} = 3V$, $I_C = 10mA$
		40	100			$V_{CE} = 3V$, $I_C = 1mA$
			50			$V_{CE} = 3V$, $I_C = 10\mu A$
Input offset current differential pair	I_{IO}		0.2	2	μA	$V_{CE} = 3V$, $I_C = 1mA$
Input offset voltage differential pair	ΔV_{BE1}		0.35	5	mV	$V_{CE} = 3V$, $I_C = 1mA$
Input offset voltage isolated transistors	ΔV_{BE2}		0.45	5	mV	$V_{CE} = 3V$, $I_C = 1mA$
Temperature coefficient of input offset voltage	$\frac{\partial \Delta V_{BE}}{\partial T}$		2		μV°C	$V_{CE} = 3V$, $I_C = 1mA$
Temperature coefficient of base emitter voltage	$\frac{\partial V_{BE(ON)}}{\partial T}$		-1.8		mV/°C	$V_{CE} = 3V$, $I_C = 1mA$
Dynamic characteristics						
Wideband noise figure	NF		3.25		dB	f = 10Hz to 10kHz $V_{CE} = 3V$, $I_C = 100\mu A$ Source resistance = 1kΩ
Forward transfer admittance	Y_{fe}		31-j1.5		mmho	
Input admittance	Y_{ie}		0.3-j0.04		mmho	f = 1MHz
Output admittance	Y_{oe}		0.001 +j0.03		mmho	$V_{CE} = 3V$, $I_C = 1mA$
Reverse transfer admittance	Y_{re}		0.000-j0.003		mmho	
Forward current transfer ratio	h_{fe}		110			
Short circuit input impedance	h_{ie}		3.5		kΩ	
Open circuit output admittance	h_{oe}		15.6		μmho	f = 1kHz
Open circuit reverse voltage transfer ratio	h_{re}		1.8×10^{-4}			$V_{CE} = 3V$, $I_C = 1mA$
Gain bandwidth product	f_T	300	500		MHz	$V_{CE} = 3V$, $I_C = 3mA$
Emitter base capacitance	C_{EB}		1.2		pF	$V_{EB} = 3V$, $I_E = 0$
Collector base capacitance	C_{OB}		0.65		pF	$V_{CB} = 3V$, $I_C = 0$
Collector substrate capacitance	C_{CI}		2.55		pF	$V_{CS} = 3V$, $I_C = 0$

NOTE 1. Typical values are for design guidance only

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified performance may be impaired.

All electrical ratings apply to individual transistors; thermal ratings apply to total package dissipation.

The isolation pin must always be negative with respect to the collectors.

Chip-to-case thermal resistance	40°C/W (DG14)
Chip-to-ambient thermal resistance	125°C/W (DG14)
	175°C/W (DP14)
Storage temperature	−55°C to +175°C (DG14)
	−55°C to +125°C (DP14)
Junction operating temperature	+175°C (DG14)
	+125°C (DP14)

$V_{CBO} = 20V$ $V_{EBO} = 6V$ $I_C = 15mA$ $I_B = 10mA$
$V_{CEO} = 15V$ $V_{CIO} = 20V$ $I_E = 15mA$

PLESSEY
Semiconductors

SL3127C

HIGH FREQUENCY NPN TRANSISTOR ARRAY

The SL3127C is a monolithic array of five high frequency low current NPN transistors in a 16 lead DIL package. The transistors exhibit typical f_Ts of 1.6GHz and wideband noise figures of 3.6dB. The SL3127C is pin compatible with the CA3127.

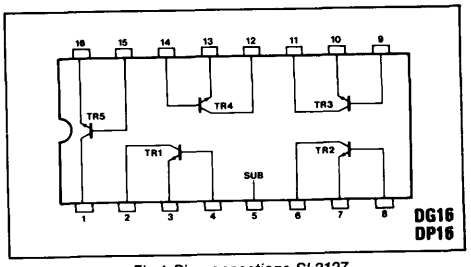


Fig.1 Pin connections SL3127

FEATURES

- f_T Typically 1.6 GHz
- Wideband Noise Figure 3.6dB
- V_{BE} Matching Better Than 5mV

APPLICATIONS

- Wide Band Amplifiers
- PCM Regenerators
- High Speed Interface Circuits
- High Performance Instrumentation Amplifiers
- High Speed Modems

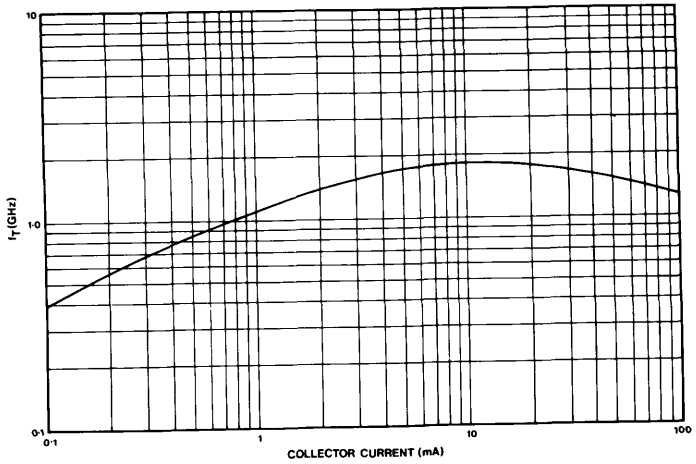


Fig. 3 Transition frequency (f_T) v. collector current (V_{CB}=2V, f=200MHz)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = 22°C \pm 2°C$

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Static characteristics						
Collector base breakdown	BV_{CBO}	20	30		V	$I_C = 10\mu A$, $I_E = 0$
Collector emitter breakdown	LV_{CEO}	15	18		V	$I_C = 1mA$, $I_B = 0$
Collector substrate breakdown (isolation)	BV_{CIO}	20	55		V	$I_C = 10\mu A$, $I_R = I_E = 0$
Base to isolation breakdown	BV_{BIO}	10	20		V	$I_B = 10\mu A$, $I_C = I_E = 0$
Base emitter voltage	V_{BE}	0.64	0.74	0.84	V	$V_{CE} = 6V$, $I_C = 1mA$
Collector emitter saturation voltage	$V_{CE(SAT)}$		0.26	0.5	V	$I_C = 10mA$, $I_B = 1mA$
Emitter base leakage current	I_{EBO}		0.1	1	μA	$V_{EB} = 4V$
Base emitter saturation voltage	$V_{BE(SAT)}$		0.95		V	$I_C = 10mA$, $I_B = 1mA$
Base emitter voltage difference, all transistors	ΔV_{BE}		0.45	5	mV	$V_{CE} = 6V$, $I_C = 1mA$
Input offset current	ΔI_B		0.2	3	μA	$V_{CE} = 6V$, $I_C = 1mA$
Temperature coefficient of ΔV_{BE}	$\frac{\partial \Delta V_{BE}}{\partial T}$		2.0		$\mu V/°C$	$V_{CE} = 6V$, $I_C = 1mA$
Temperature coefficient of V_{BE}	$\frac{\partial V_{BE}}{\partial T}$		-1.6		mV/°C	$V_{CE} = 6V$, $I_C = 1mA$
Static forward current ratio	H_{FE}	35	95			$V_{CE} = 6V$, $I_C = 5mA$
		35	100			$V_{CE} = 6V$, $I_C = 0.1mA$
		40	100			$V_{CE} = 6V$, $I_C = 1mA$
Collector base leakage	I_{CBO}		0.3		nA	$V_{CB} = 16V$
Collector isolation leakage	I_{CIO}		0.6		nA	$V_{CI} = 20V$
Base isolation leakage	I_{BIO}		100		nA	$V_{BI} = 5V$
Emitter base capacitance	C_{EB}		0.4		pF	$V_{EB} = 0V$
Collector base capacitance	C_{CB}		0.4		pF	$V_{CB} = 0V$
Collector isolation capacitance	C_{CI}		0.8		pF	$V_{CI} = 0V$
Dynamic characteristics						
Transition frequency	f_T		1.6		GHz	$V_{CE} = 6V$, $I_C = 5mA$
Wideband noise figure	NF		3.6		dB	$f = 60MHz$, $V_{CC} = 6V$, $I_C = 2mA$, $R_S = 200\Omega$
Knee of 1/f noise curve			1		kHz	

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life maybe shortened or specified parameters may be degraded.

All electrical ratings apply to individual transistors. Thermal ratings apply to the total package.

The isolation pin (substrate) must be connected to the most negative voltage applied to the package to maintain electrical isolation.

$V_{CB} = 20$ volt
$V_{EB} = 4.0$ volt
$V_{CE} = 15$ volt
$V_{CI} = 20$ volt
$I_C = 20$ mA
Maximum individual transistor dissipation 200 mWatt
Storage temperature −55°C to 150°C
Max junction temperature 150°C

Package thermal resistance (°C/watt):−

Package Type	DG16	DP16
Chip to case	40	
Chip to ambient	120	180

NOTE:
If all the power is being dissipated in one transistor, these thermal resistance figures should be increased by 100° C/watt.

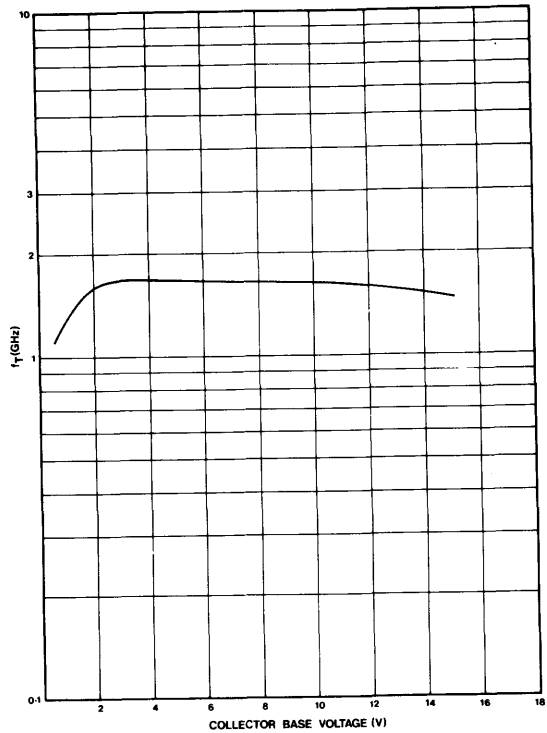


Fig. 4 Transition frequency (f_T) v. collector base voltage
(I_C = 5mA, Frequency = 200MHz)

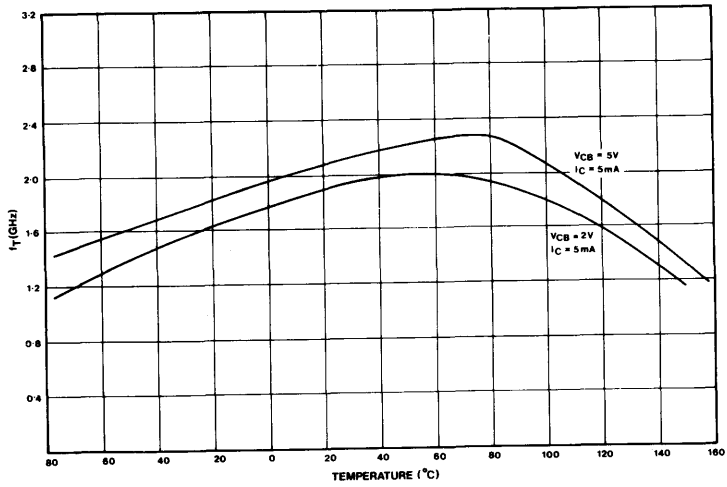


Fig. 5 Variation of transition frequency (f_T) with temperature

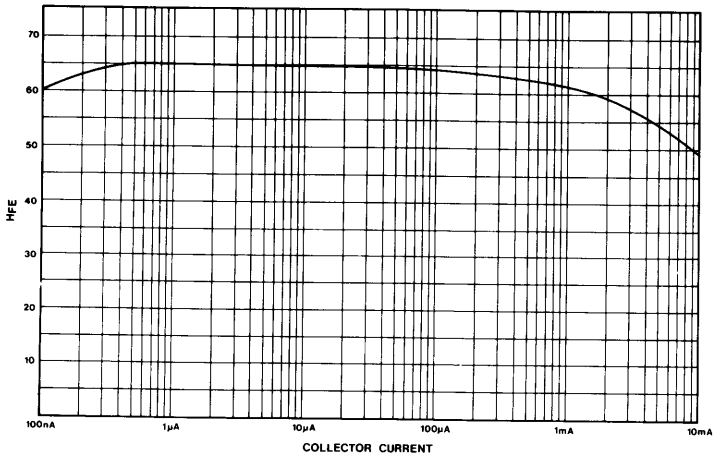


Fig. 6 DC current gain v. collector current

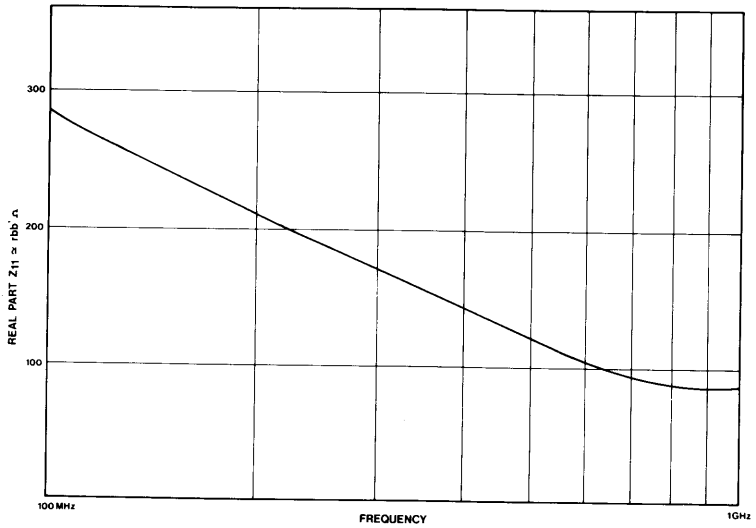


Fig. 7 Z_{11} (derived from scattering parameters) v. frequency ($Z_{11} \simeq r_{66'}$)

PLESSEY
Semiconductors

SL3145C,E

1.2GHz HIGH FREQUENCY NPN TRANSISTOR ARRAYS

The SL3145C is a monolithic array of five high frequency low current NPN transistors. The SL3145C consists of 3 isolated transistors and a differential pair in a 14 lead DIL package. The transistors exhibit typical f_{TS} of 1.6GHz and wideband noise figures of 3.0dB. The device is pin compatible with the SL3045C. The SL3145E has guaranteed C_{CB} and f_T figures.

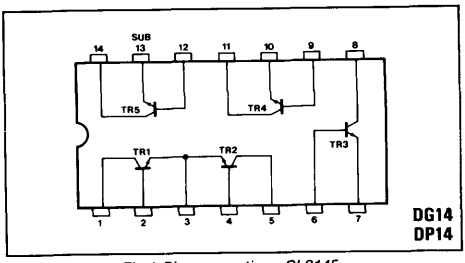


Fig.1 Pin connections SL3145

FEATURES

- f_T Typically 1.6 GHz
- Wideband Noise Figure 3.0dB
- V_{BE} Matching Better Than 5mV

APPLICATIONS

- Wide Band Amplifiers
- PCM Regenerators
- High Speed Interface Circuits
- High Performance Instrumentation Amplifiers
- High Speed Modems

Ordering Information	
SL3145C-DG	Ceramic
SL3145C-DP	Plastic
SL3145E-DP	Plastic

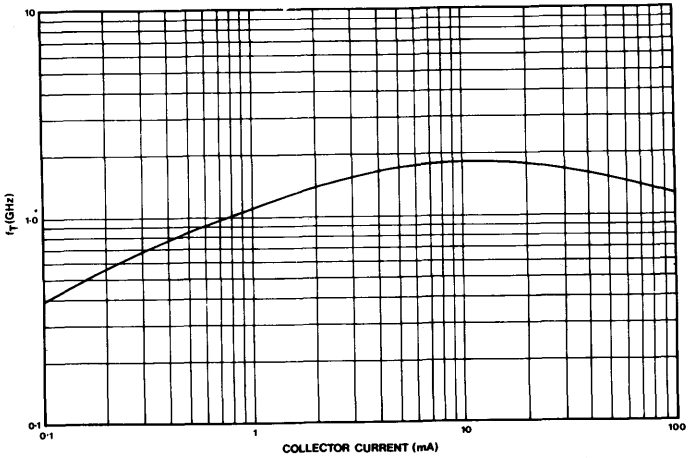


Fig.2 Transition frequency (f_T) v. collector current (V_{CB} = 2V, f = 200MHz)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 22°C ± 2°C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Static characteristics						
Collector base breakdown	BV_{CBO}	20	30		V	I_C = 10μA,I_E = 0
Collector emitter breakdown	LV_{CEO}	15	18		V	I_C = 1mA,I_B = 0
Collector substrate breakdown (isolation)	BV_{CIO}	20	55		V	I_C = 10μA,I_R = I_E = 0
Base to isolation breakdown	BV_{BIO}	10	20		V	I_B = 10μA,I_C = I_E = 0
Base emitter voltage	V_{BE}	0.64	0.74	0.84	V	V_{CE} = 6V,I_C = 1mA
Collector emitter saturation voltage	$V_{CE(SAT)}$		0.26	0.5	V	I_C = 10mA,I_B = 1mA
Emitter base leakage current	I_{EBO}		0.1	1	μA	V_{EB} = 4V
Base emitter saturation voltage	$V_{BE(SAT)}$		0.95		V	I_C = 10mA,I_B = 1mA
Base emitter voltage difference, all transistors except TR1,TR2	ΔV_{BE}		0.45	5	mV	V_{CE} = 6V,I_C = 1mA
Base emitter voltage difference TR1, TR2	ΔV_{BE}		0.35	5	mV	V_{CE} = 6V,I_C = 1mA
Input offset current (except for TR1, TR2)	ΔI_B		0.2	3	μA	V_{CE} = 6V,I_C = 1mA
Input offset current TR1, TR2	ΔI_B		0.2	2	μA	V_{CE} = 6V,I_C = 1mA
Temperature coefficient of ΔV_{BE}	$\frac{\partial \Delta V_{BE}}{\partial T}$		2.0		μV/°C	
Temperature coefficient of V_{BE}	$\frac{\partial V_{BE}}{\partial T}$		-1.6		mV/°C	V_{CE} = 6V,I_C = 1mA
Static forward current ratio	H_{FE}	40	100			V_{CE} = 6V,I_C = 1mA
Collector base leakage	I_{CBO}		0.3		nA	V_{CB} = 16V
Collector isolation leakage	I_{CIO}		0.6		nA	V_{CI} = 20V
Base isolation leakage	I_{BIO}		100		nA	V_{BI} = 5V
Emitter base capacitance	C_{EB}		0.4		pF	V_{EB} = 0V
Collector base capacitance						
SL3145C	C_{CB}		0.4		pF	V_{CB} = 0V
SL3145E			0.4	1.1	pF	V_{CB} = 0V
Collector isolation capacitance	C_{CI}		0.8		pF	V_{CI} = 0V
Dynamic characteristics						
Transition frequency						
SL3145C	f_T		1.6		GHz	V_{CE} = 6V,I_C = 5mA
SL3145E		1.2			GHz	V_{CE} = 6V,I_C = 10mA
Wideband noise frequency	NF		3.0		dB	V_{CE} = 2V,R_S = 1kΩ I_C = 100μA,f = 60MHz
Knee of 1/f noise curve			1		kHz	V_{CE} = 6V,R_S = 200Ω I_C = 2mA

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life maybe shortened or specified parameters may be degraded.

All electrical ratings apply to individual transistors. Thermal ratings apply to the total package.

The isolation pin (substrate) must be connected to the most negative voltage applied to the package to maintain electrical isolation.

V_{CB} = 20 volt
V_{EB} = 4.0 volt
V_{CE} = 15 volt
V_{CI} = 20 volt
I_C = 20 mA
Maximum individual transistor dissipation 200 mWatt
Storage temperature −55°C to 150°C
Max junction temperature 150°C

Package thermal resistance (°C/watt):−

Package Type	DG14	DP14
Chip to case	40	
Chip to ambient	125	180

NOTE:
If all the power is being dissipated in one transistor, these thermal resistance figures should be increased by 100° C/watt.

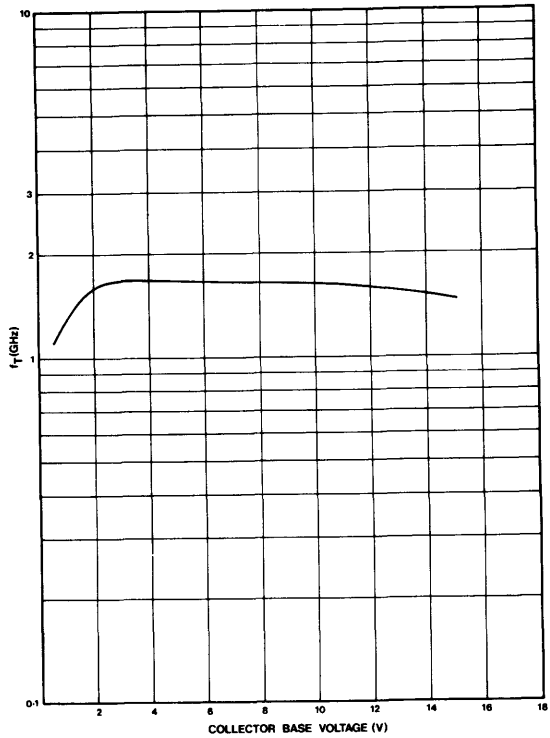


Fig.3 Transition frequency (f_T) v. collector base voltage (I_C = 5mA, frequency = 200MHz)

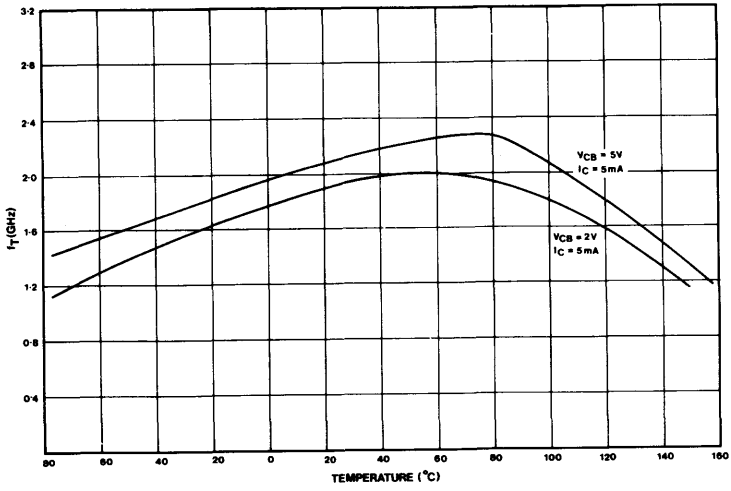


Fig.4 Variation of transition frequency (f_T) with temperature

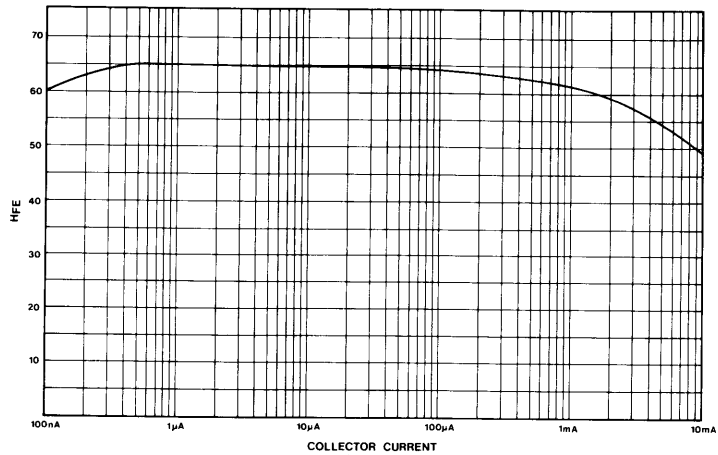


Fig.5 DC current gain v. collector curent

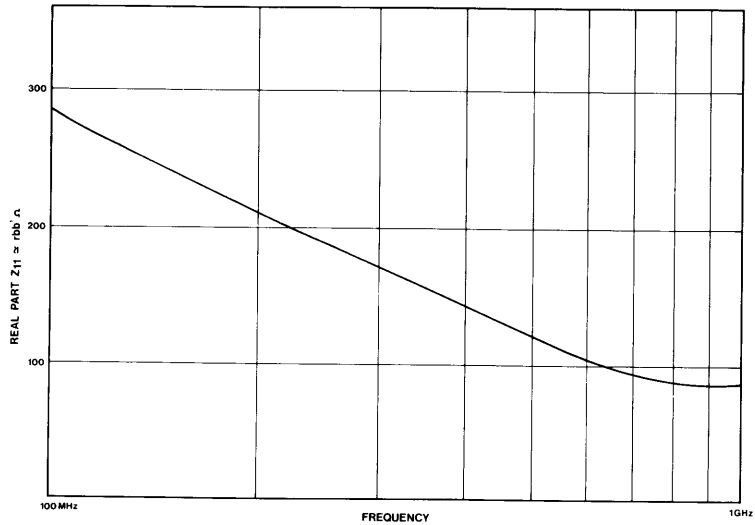


Fig.6 Z_{11} (derived from scattering parameters) v. frequency ($Z_{11} \simeq r_{66'}$)

PLESSEY
Semiconductors

SL6270C

GAIN CONTROLLED PREAMPLIFIER

The SL6270C is a silicon integrated circuit combining the functions of audio amplifier and voice operated gain adjusting device (VOGAD).

It is designed to accept signals from a low sensitivity microphone and to provide an essentially constant output signal for a 60dB range of input. The dynamic range, attack and decay times are controlled by external components.

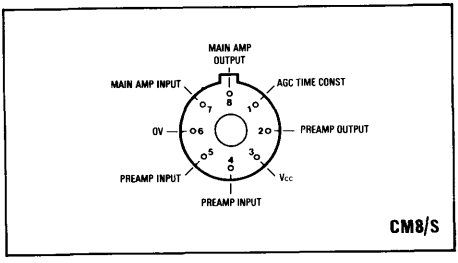


Fig. 1 Pin connections, SL6270C – CM (bottom view)

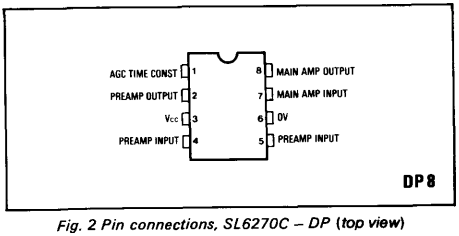


Fig. 2 Pin connections, SL6270C – DP (top view)

FEATURES

- Constant Output Signal
- Fast Attack
- Low Power Consumption
- Simple Circuitry

APPLICATIONS

- Audio AGC Systems
- Transmitter Overmodulation Protection
- Tape Recorders

QUICK REFERENCE DATA

- Supply Voltage: 4.5V to 10V
- Voltage Gain: 52dB

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: −55°C to +125°C

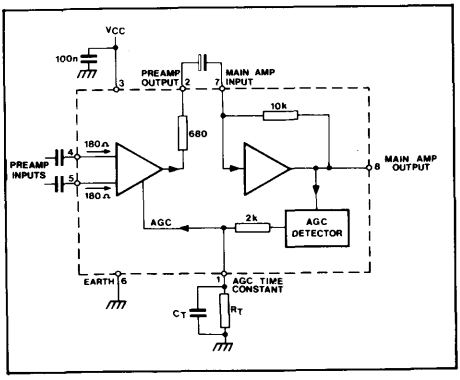
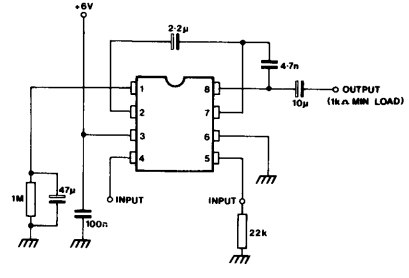


Fig. 3 SL6270C block diagram

ELECTRICAL CHARACTERISTICS

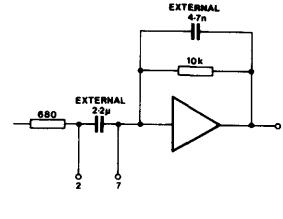
Test conditions (unless otherwise stated):
Supply voltage Vcc: 6V
Input signal frequency: 1kHz
Ambient temperature: −30°C to +85°C
Test circuit shown in Fig. 4

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5	10	mA	
Input impedance		150		Ω	Pin 4 or 5
Differential input impedance		300		Ω	
Voltage gain	40	52		dB	72μV rms input pin 4
Output level	55	90	140	mV rms	4mV rms input pin 4
THD		2	5	%	90mV rms input pin 4



N.B. If input not AC coupled the resistance between pins 4 and 5 must be less than 10 ohms.

Fig. 4 SL6270C test and application circuit



$$\text{Voltage gain} = \frac{10k\Omega}{680\Omega}$$

Upper frequency response 10kΩ/4.7nF = 3kHz
Lower frequency response 680Ω/2.2μF = 300Hz

Fig. 5 SL6270C frequency response

APPLICATION NOTES

Voltage gain

The input to the SL6270C may be single ended or differential but must be capacitor coupled. In the single-ended mode the signal can be applied to either input, the remaining input being decoupled to ground. Input signals of less than a few hundred microvolts rms are amplified normally but as the input level is increased the AGC begins to take effect and the output is held almost constant at 90mV rms over an input range of 50dB.

The dynamic range and sensitivity can be reduced by reducing the main amplifier voltage gain. The connection of a 1k resistor between pins 7 and 8 will reduce both by approximately 20dB. Values less than 680Ω are not advised.

Frequency response

The low frequency response of the SL6270C is determined by the input, output and coupling capacitors. Normally the coupling capacitor between pins 2 and 7 is chosen to give a −3dB point at 300Hz, corresponding to 2.2μF, and the other capacitors are chosen to give a response to 100Hz or less.

The SL6270C has an open loop upper frequency response of a few MHz and a capacitor should be connected between pins 7 and 8 to give the required bandwidth.

Attack and decay times

Normally the SL6270C is required to respond quickly by holding the output level almost constant as the input is increased. This 'attack time', the time taken for the output to return to within 10% of the original level following a 20dB increase in input level, will be approximately 20ms with the circuit of Fig. 4. It is determined by the value of the capacitor connected between pin 1 and ground and can be calculated approximately from the formula:

$$\text{Attack time} = 0.4\text{ms}/\mu\text{F}$$

The decay time is determined by the discharge rate of the capacitor and the recommended circuit gives a decay rate of 20dB/second. Other values of resistance between pin 1 and ground can be used to obtain different results.

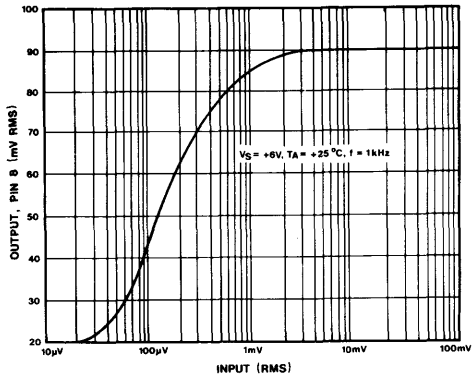


Fig. 6 Voltage gain (single ended input) (typical)

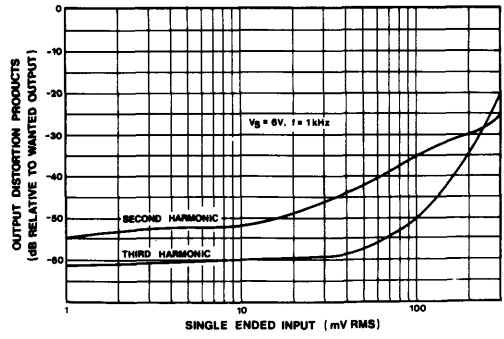


Fig. 7 Overload characteristics (typical)

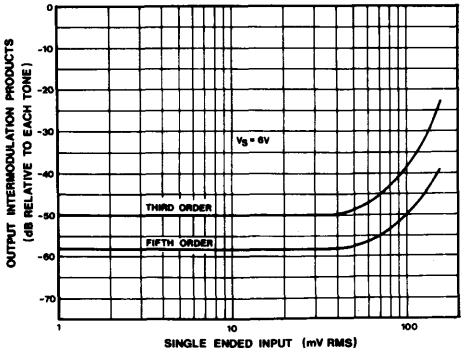


Fig. 8 Typical Intermodulation distortion (1.55 and 1.85kHz tones)

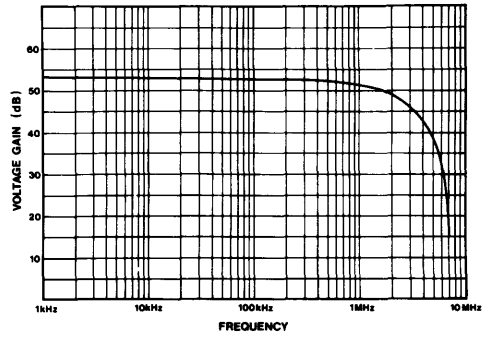


Fig. 9 Open loop frequency response (typical)

PLESSEY
Semiconductors

SL6310C

SWITCHABLE AUDIO AMPLIFIER

The SL6310C is a low power audio amplifier which can be switched off by applying a mute signal to the appropriate pin. Despite the low quiescent current consumption of 5mA (only 0.6mA when muted) a minimum output power of 400mW is available into an 8Ω load from a 9V supply.

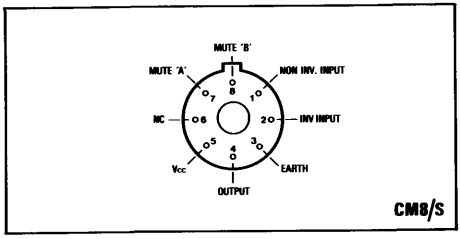


Fig. 1 Pin connections, SL6310C — CM (bottom view)

FEATURES

- Can be Muted with High or Low State Inputs
- Operational Amplifier Configuration
- Works Over Wide Voltage Range

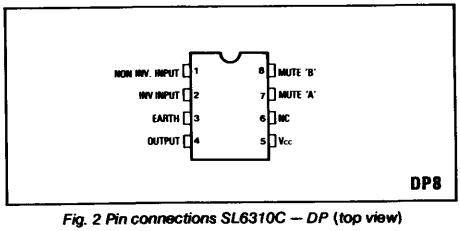


Fig. 2 Pin connections SL6310C — DP (top view)

APPLICATIONS

- Audio Amplifier for Portable Receivers
- Power Op. Amp
- High Level Active Filter

QUICK REFERENCE DATA

- Supply Voltage: 4.5V to 13.6V
- Voltage Gain: 70dB
- Output into 8Ω on 9V Supply: 400mW

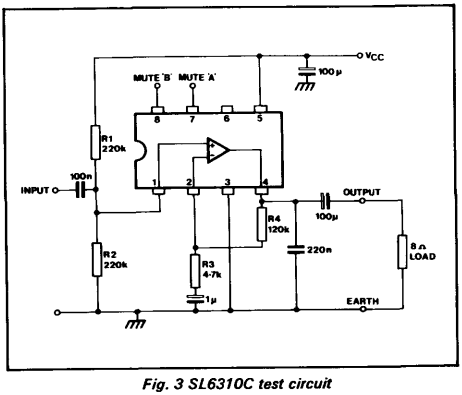


Fig. 3 SL6310C test circuit

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 15V
Storage temperature: −55°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage Vcc: 9V
Ambient temperature: −30°C to +85°C
Mute facility: Pins 7 and 8 open circuit

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5.0	7.5	mA	
Supply current muted (A)		0.55	1	mA	Pin 7 via 100k to earth
Supply current muted (B)		0.6	0.9	mA	Pin 8 = Vcc
Input offset voltage		2	20	mV	Rs ⩽ 10k
Input offset current		50	500	nA	
Input bias current (Note 1)		0.2	1	μA	
Voltage gain	40	70		dB	
Input voltage range		2.1		V	Vcc = 4.5V
		10.6		V	Vcc = 13V
CMRR	40	60		dB	Rs ⩽ 10k
Output power	400	500		mW	RL = 8Ω
THD		0.4	3	%	POUT = 400mW, Gain = 28dB

NOTE
1. The input bias current flows **out** of pins 1 and 2 due to PNP input stage

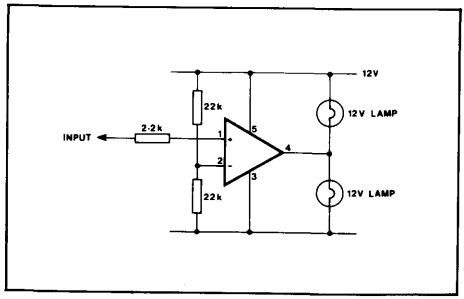


Fig. 4 SL6310C lamp driver

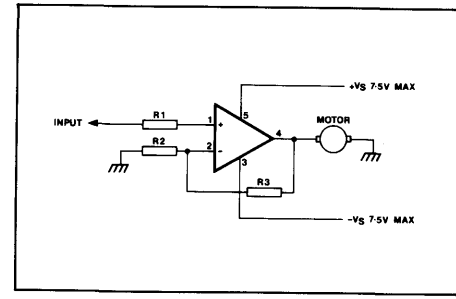


Fig. 5 SL6310C servo amplifier

OPERATING NOTES

Mute facility
The SL6310C has two mute control pins to allow easy interfacing to inputs of high or low levels. Mute control 'A', pin 7, is left open circuit or connected to a voltage within one volt of Vcc (via a 100kΩ resistor) for normal operation. When the voltage on pin 7 is reduced to within 1 volt of earth (via a 100kΩ resistor) the SL6310C is muted.

Mute control 'B', pin 8, is left open circuit or connected to a voltage less than 1 volt for normal operation: a voltage greater than 2.5V on pin 8 mutes the device. The input resistance at pin 8 is around 100kΩ and is suitable for interfacing with CMOS.

Only one mute control pin may be used at any time; the unused pin must be left open circuit.

Audio amplifier
As the SL6310C is an operational amplifier it is easy to obtain the voltage gain and frequency response required. To keep the input impedance high it is wise to feed the signal to the non-inverting input as shown in Fig. 3. In this example the input impedance is approximately 100kΩ. The voltage gain is determined by the ratio (R3 + R4)/R3 and should be between 3 and 30 for best results. The capacitor in series with R3, together with the input and output coupling capacitors, determines the low frequency rolloff point. The upper frequency limit is set by the device but can be restricted by connecting a capacitor across R4.

The output and power supply decoupling capacitors have to carry currents of several hundred milliamps and should be rated accordingly.

Applications include hand-held radio equipment, hi-fi headphone amplifiers and line drivers.

Operational amplifier
It is impossible to list all their application possibilities in a single data sheet but the SL6310C offers considerable advantages over conventional devices in high output current applications such as lamp drivers (Fig. 4) and servo amplifiers (Fig. 5).

Buffer and output stages for signal generators are another possibility together with active filter sections requiring a high output current.

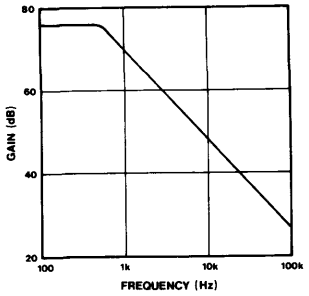


Fig. 6 Gain v frequency

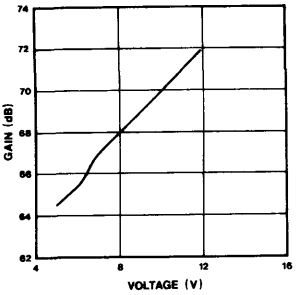


Fig. 7 Gain v. supply voltage

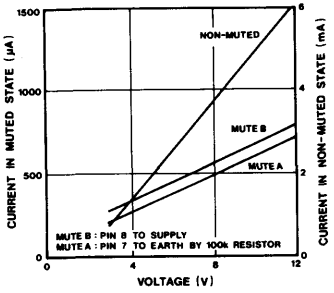


Fig. 8 Supply current v. supply voltage

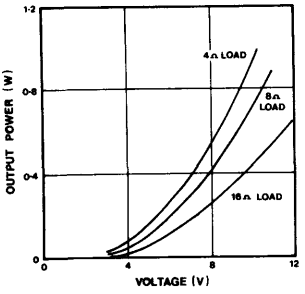


Fig. 9 Output power v. supply voltage at 5% (max) distortion

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JUN 82
ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

SL6440A&C

HIGH LEVEL MIXER

The SL6440 is a double balanced mixer intended for use in radio systems up to 150MHz. A special feature of the circuit allows external selection of the DC operating conditions by means of a resistor connected between pin 11 (bias) and Vcc. When biased for a supply current of 50mA the SL6440 offers a 3rd order intermodulation intercept point of typically +30dBm, a value previously unobtainable with integrated circuits. This makes the device suitable for many applications where diode ring mixers had previously been used and offers the advantages of a voltage gain, low local oscillator drive requirement and superior isolation.

The SL6440C (in a 16-lead DIL plastic package) is specified for operation from -30°C to +85°C; the SL6440A (in ceramic) has a military temperature range specification.

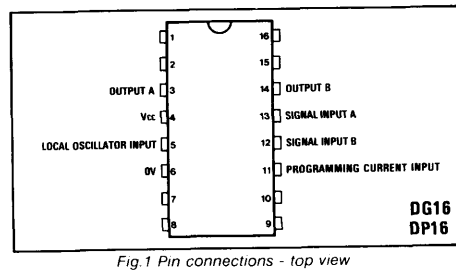

Fig.1 Pin connections - top view

FEATURES

- +30dBm Input Intercept Point
- +15dBm Compression Point (1dB)
- Programmable Performance
- -55°C to +125°C Temperature Range

APPLICATIONS

- Mixers in Radio Transceivers
- Phase Comparators
- Modulators

ABSOLUTE MAXIMUM RATINGS

Supply voltage and output pins: 15V
Power dissipation (package limitation): 1200mW
(Derate above 25° C: 8mW/° C)
Storage temperature range: -65° C to +150° C
Programming current into pin 11: 50mA

PACKAGE THERMAL DATA - BOTH PACKAGES

Thermal resistance: Junction-Ambient: 125° C/W
Junction-Case: 40° C/W
Time constant: Junction-Ambient: 1.9 mins.
Max. chip temperature: 150° C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{cc1} = 12V; V_{cc2} = 10V; I_p = 25mA; T_{amb} = -55°C to +125°C (SL6440A), -30°C to +85°C (SL6440C)
Local oscillator input level = 0dBm; Test circuit Fig. 2.

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Signal frequency 3dB point	100	150		MHz	
Oscillator frequency 3dB point	100	150		MHz	
3rd order input intercept point		+30		dBm	
Third order intermodulation distortion		-60		dB	Two 0dBm input
Second order intermodulation distortion		-75		dB	Signals
1dB compression point		15		dBm	V_{cc1} = 15V V_{cc2} = 12V
		12		dBm	V_{cc1} = 12V V_{cc2} = 10V
Noise figure		11		dB	Fig.8 test circuit
Conversion gain		-1		dB	50Ω load Fig.2
Carrier leak to signal input	-40			dB	Test circuit Fig.8
Level of carrier at IF output		-25		dBm	See applications information
Supply current		7		mA	I_p = 0
Supply current (total from V_{cc1} & V_{cc2})		60		mA	
Local oscillator input	100	250	500	mVrms	I_p = 35mA
Local oscillator input impedance		1.5		kΩ	
Signal input impedance		500		Ω	Single ended
		1000		Ω	Differential

NOTE Supply current in Pin 3 is equal to that in Pin 14 and is equal to I_p. See over. $V_{pin11} \approx 3\ V_{be} \approx 2.1V$

CIRCUIT DESCRIPTION

The SL6440 is a high level mixer designed to have a linear RF performance. The linearity can be programmed using the I_P pin (11).

The output pins are open collector outputs so that the conversion gain and output loads can be chosen for the specific application.

Since the outputs are open collectors they should be returned to a supply V_{CC1} through a load.

The choice of V_{CC1} is important since it must be ensured that the voltage on pins 3 and 14 is not low enough to saturate the output transistors and so limit the signal swing unnecessarily. If the voltage on pins 3 and 14 is always greater than V_{CC2} the outputs will not saturate. The output frequency response will reduce as the output transistors near saturation.

Minimum V_{CC1} = $(I_P \times RL) + V_S + V_{CC2}$
where I_P = programmed current
RL = DC load resistance
V_S = max signal swing at output
if the signal swing is not known:
minimum V_{CC1} = $2 (I_P \times RL) + V_{CC2}$

In this case the signal will be limiting at the input before the output saturates.

The device has a separate supply (V_{CC2}) for the oscillator buffer (pin 4).

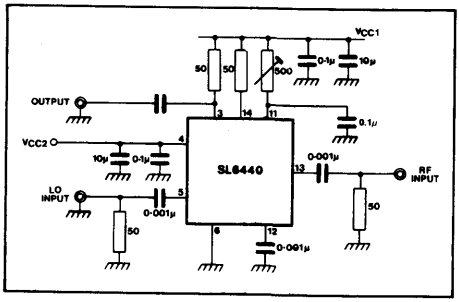

Fig.2 Typical application and test circuit

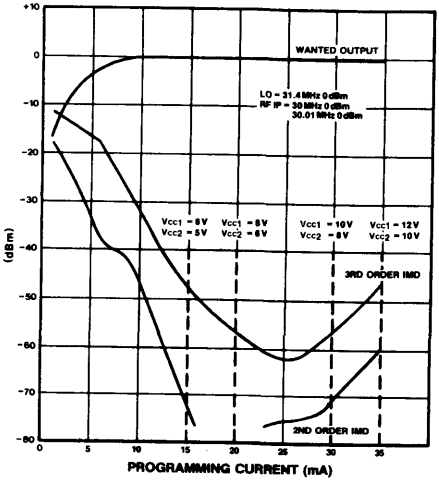

Fig.4 Intermodulation v. programming current

The current (I_P) programmed into pin 11 can be supplied via a resistor from V_{CC1} or from a current source.

The conversion gain is equal to

$$GdB = 20 \text{ Log } \frac{RL\ I_P}{56.6\ I_P + 0.0785} \text{ for single-ended output}$$

$$GdB = 20 \text{ Log } \frac{2\ RL\ I_P}{56.6\ I_P + 0.0785} \text{ for differential output}$$

Device dissipation is calculated using the formula

mW diss = $2\ I_P\ V_O + V_P\ I_P + V_{CC2}$ Diss
where V_O = voltage on pin 3 or pin 14
V_P = voltage on pin 11
I_P = programming current (mA)
V_{CC2} Diss = dissipation obtained from graph(Fig.5)

As an example Fig. 7 shows typical dissipations assuming V_{CC1} and V_O are equal. This may not be the case in practice and the device dissipation will have to be calculated for any particular application.

Fig. 4 shows the intermodulation performance against I_P. The curves are independent of V_{CC1} and V_{CC2} but if V_{CC1} becomes too low the output signal swing cannot be accommodated, and if V_{CC2} becomes too low the circuit will not provide enough drive to sink the programmed current. Examples are shown of performance at various supply voltages.

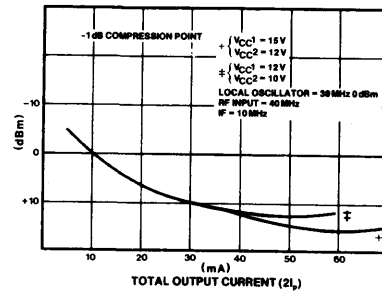

Fig.3 Compression point v. total output current

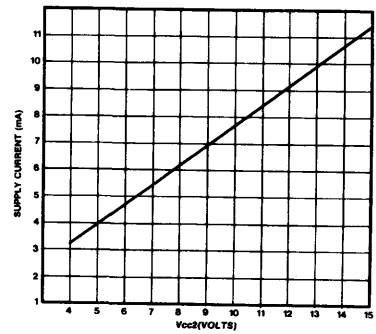

Fig.5 Supply current v. V_{CC2} (I_P = 0)

The current in pin 14 is equal to the current in pin 3 which is equal to the current in pin 11.

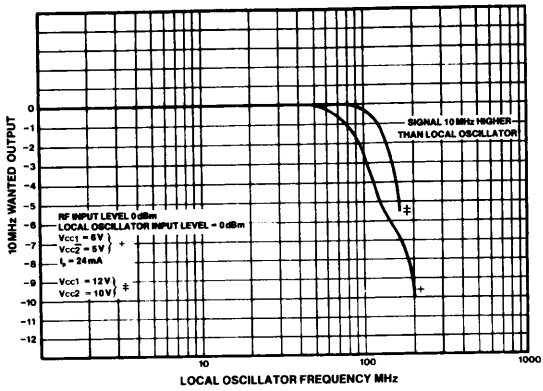

Fig.6 Frequency response at constant output IF

APPLICATIONS

The SL6440 can be used with differential or single-ended inputs and outputs. A balanced input will give better carrier leak. The high input impedance allows step-up transformers to be used if desired, whilst high output impedance allows a choice of output impedance and conversion gain.

Fig. 2 shows the simplest application circuit. The input and output are single-ended and I_P is supplied from $V_{CC}1$ via a resistor. Increasing RL will increase the conversion gain, care being taken to choose a suitable value for $V_{CC}1$.

Fig. 8 shows an application with balanced input, for improved carrier leak, and balanced output for increased conversion gain. A lower $V_{CC}1$ giving lower device dissipation can be used with this arrangement.

Further Applications information is available. Request AN1007 and AN1009.

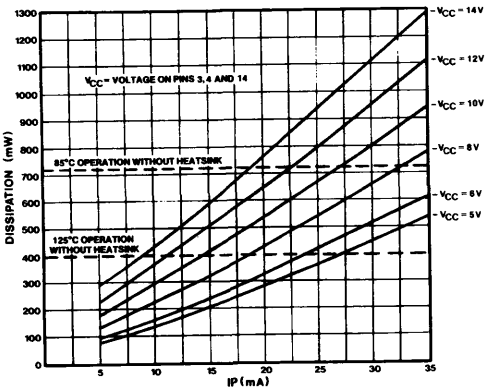

Fig.7 Device dissipation v. I_P

DESIGN PROCEDURE

1. Decide on input configuration using local oscillator data. If using transformer on input, decide on ratio from noise considerations.
2. Decide on output configuration and value of conversion gain required.
3. Decide on value of I_P and $V_{CC}2$ using intermodulation and compression point graphs.
4. Using values of conversion gain, $V_{CC}2$, load and I_P already chosen, decide on value of $V_{CC}1$.
5. Calculate device dissipation and decide whether heatsink is required from maximum operating temperature considerations.

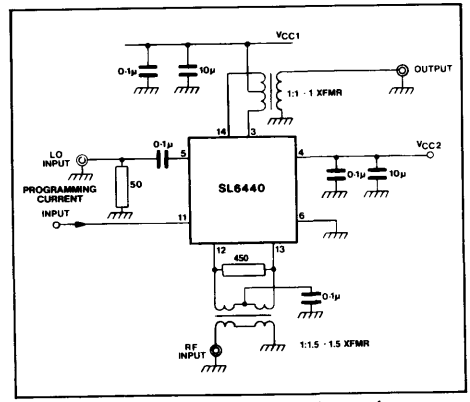

Fig.8 Typical application circuit for highest performance

PLESSEY
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SL6601C

LOW POWER IF/AF PLL CIRCUIT FOR NARROW BAND FM

The SL6601 is a straight through or single conversion IF amplifier and detector for FM radio applications. Its minimal power consumption makes it ideal for hand held and remote applications where battery conservation is important. Unlike many FM integrated circuits, the SL6601 uses an advanced phase locked loop detector capable of giving superior signal-to-noise ratio with excellent co-channel interference rejection, and operates with an IF of less than 1MHz. Normally the SL6601 will be fed with an input signal of up to 17MHz: there is a crystal oscillator and mixer for conversion to the IF amplifier, a PLL detector and squelch system.

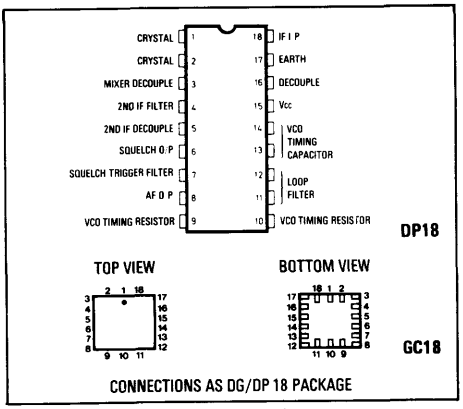

Fig.1 Pin connections

FEATURES

- High Sensitivity: 2μV Typical
- Low Power: 2·3mA Typical at 7V
- Advanced PLL Detector
- Available in Miniature 'Chip Carrier' Package
- 100% Tested for SINAD

APPLICATIONS

- Low Power NBFM Receivers
- FSK Data Equipment
- Cellular Radio Telephones

QUICK REFERENCE DATA

- Supply Voltage 7V
- 50dB S/N Ratio

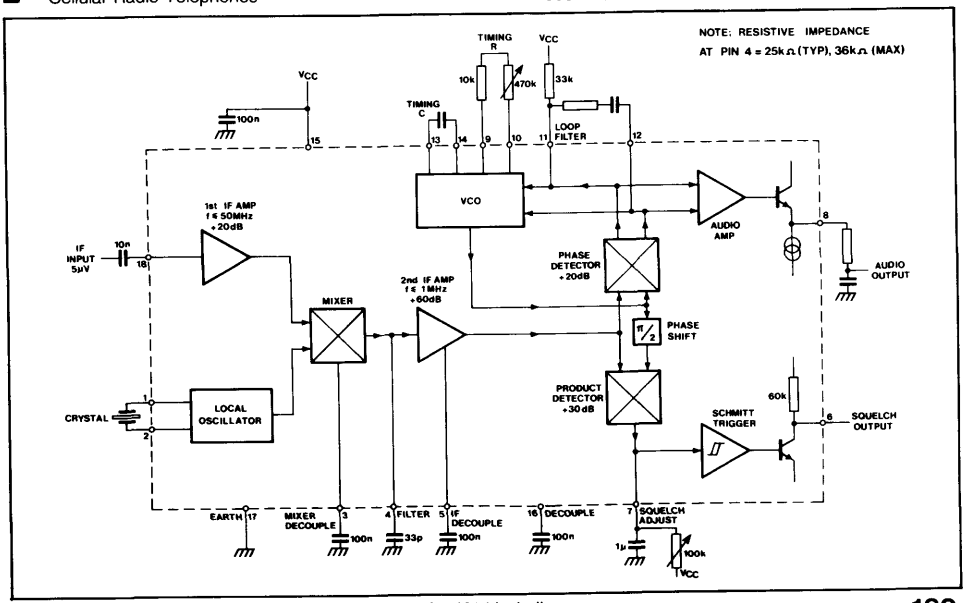

Fig.2 SL6601 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage V_{CC} : 7V

Input signal frequency: 10.7MHz, frequency modulated with a 1kHz tone with a ±2.5kHz frequency deviation

Ambient temperature: -30°C to +85°C; IF = 100kHz; AF bandwidth = 15kHz

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		2.3	2.7	mA	
Input impedance	100		300	Ω	Source impedance = 200Ω
Input capacity	0.5	2.0	3.5	pF	
Maximum input voltage level	0.5			V rms	At pin 18
Sensitivity	5	2		μV rms	At pin 18 for S + N/N = 20dB
Audio output	35	90	140	mV rms	
Audio THD		1.3	3.0	%	1mV rms input at pin 18
S + N/N	30	50		dB	1mV rms input at pin 18
AM rejection	30	Note 1		dB	100μV rms input at pin 18, 30% AM
Squelch low level		0.2	0.5	V dc	20μV rms input at pin 18
Squelch high level	6.5	6.9		V dc	No input
Squelch hysteresis		1	6	dB	3μV input at pin 18
Noise figure		6		dB	50Ω source
Conversion gain		30		dB	Pin 18 to pin 4
Input gain compression		100		μV rms	Pin 18 to pin 4, 1dB compression
Squelch output load	250			kΩ	
Input voltage range	80	100		dB	At pin 8; above 20dB S + N/N
3rd order intercept point (input)		-38		dBm	Input pin 18, output pin 4
VCO frequency					
Grade 1	85		100	kHz	390pF timing capacitor } No input
Grade 2	95		110	kHz	390pF timing capacitor } No input
Grade 3	105		120	kHz	390pF timing capacitor } No input
Source impedance (pin 4)		25	40	kΩ	
AF output impedance		4	10	kΩ	
Lock-in dynamic range	±8			kHz	20μV to 1mV rms at pin 18
External LO drive level	50		250	mV rms	At pin 2
Crystal ESR			25	Ω	10.8MHz

APPLICATION NOTES

IF Amplifiers and Mixer

The SL6601 can be operated either in a 'straight through' mode with a maximum recommended input frequency of 800kHz or in a single conversion mode with an input frequency of 50MHz maximum and an IF of 100kHz or ten times the peak deviation, whichever is the larger. The crystal oscillator frequency can be equal to either the sum or difference of the two IF's; the exact frequency is not critical.

The circuit is designed to use series resonant fundamental crystals between 1 and 17MHz.

When a suitable crystal frequency is not available a fundamental crystal of one third of that frequency may be used, with some degradation in performance.
recommended level is 70mV rms and the unused pin should be left O/C. The input is AC coupled via a 0.01μF capacitor.

A capacitor connected between pin 4 and ground will shunt the mixer output and limit the frequency response of the mixer output and limit the frequency response of the input signal to the second IF amplifier. A value of 33pF is advised when the second IF frequency is 100kHz; 6.8pF is advised for 455kHz.

Phase Locked Loop

The Phase Locked Loop detector features a voltage controlled oscillator with nominal frequency set by an external capacitor according to the formula $(\frac{f}{35})$pF, where f is the VCO frequency in MHz. The nominal frequency may differ from the theoretical but there is provision for a fine frequency adjustment by means of a variable resistor between the VCO output pins; a value of 470k has negligible effect while 6.8k (recommended minimum value) increases the frequency by approximately 20%.

Care should be taken to ensure that the free running VCO frequency is correct; because the VCO and limiting IF amplifier output produce square waves, it is possible to obtain lock with the VCO frequency fractionally related to the IF, e.g. IF = 100kHz, VCO = 150kHz. This condition can produce good SINAD ratios but poor squelch performance.

The loop filter is connected between pins 11 and 12; a 33k resistor is also required between pin 11 and V_{CC}.

The values of the filter resistor R2 and capacitor C1 must be chosen so that the natural loop frequency and damping factor are suitable for the FM deviation and modulation bandwidth required. The recommended values for various conditions are tabulated below:

Centre frequency kHz	Deviation kHz	Resistor kΩ	Capacitor pF
100	5	6.2	2200
100	10	5.6	1800
455	5	4.7	1500
455	10	3.9	1200

Note that the values of loop filter are not critical and in many cases may be omitted.

The AF output voltage depends upon the % deviation and so, for a given deviation, output is inversely proportional to centre frequency. As the noise is constant, the signal to noise ratio is also inversely proportional to centre frequency.

VCO Frequency Grading

The SL6601 is supplied in 3 selections of VCO centre frequency. This frequency is measured with a 390pF timing capacitor and no input signal.

Devices are coded 'SL6601C' and a '/1', '/2', '/3' to indicate the selection.

Frequency tolerances are:

/1 85 - 100kHz
/2 95 - 110kHz
/3 105 - 120kHz

Note that orders cannot be accepted for any particular selection, but all devices in a tube will be the same selection.

Squelch Facility

When inputs to the product detector differ in phase a series of current pulses will flow out of pin 7. The feature can be used to adjust the VCO; when a 1mV unmodulated input signal is applied to pin 18 the VCO frequency should be trimmed to maximise the voltage on pin 7.

The squelch level is adjusted by means of a preset variable resistor between pin 7 and Vcc to set the output signal to noise ratio at which it is required to mute the output. The capacitor between pin 7 and ground determines the squelch attack time. A value between 10nF and 10μF can be chosen to give the required characteristics.

Operation at signal to noise ratios outside the range 5-18dB is not recommended. Where the 'front end' noise is high (because of very high front end gain) the squelch may well never operate. This effect can be obviated by sensible receiver gain distribution.

The load on the squelch output (pin 6) should not be less than 250kΩ. Reduction of the load below this level leads to hysteresis problems in the squelch circuit.

The use of an external PNP transistor allows hysteresis to be increased. See Fig.3. The use of capacitors greater than 1000pF from pin 6 to ground is not recommended.

Outputs

High speed data outputs can be taken direct from pins 11 and 12 but normally for audio applications pin 8 is used. A filter network will be needed to restrict the audio bandwidth and an RC network consisting of 4.7kΩ and 4.7nF may be used.

Layout Techniques and Alignment

The SL6601 is not critical in PCB layout requirements except in the 'straight through' mode. In this mode, the input components and circuits should be isolated from the VCO components, as otherwise the VCO will attempt to 'lock' to itself, and the ultimate signal to noise ratio will suffer.

The recommended method of VCO adjustment is with a frequency measurement system on pin 9. The impedance must be high, and the VCO frequency is adjusted with no input signal.

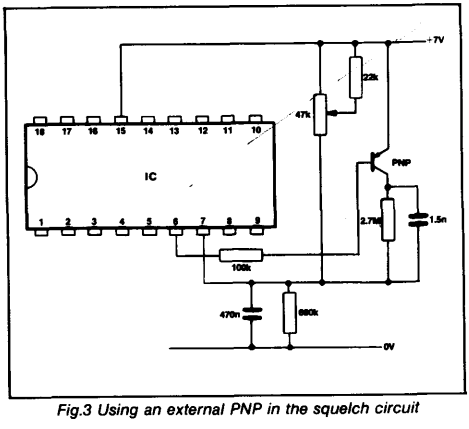

Fig.3 Using an external PNP in the squelch circuit

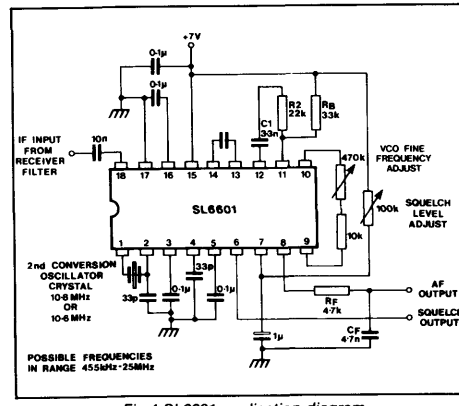

Fig.4 SL6601 application diagram (1st IF = 10.7MHz, 2nd IF = 100kHz)

TYPICAL CHARACTERISTICS

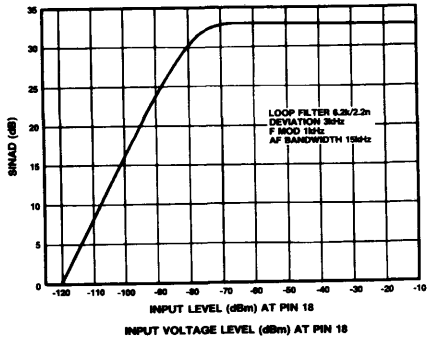

Fig.5 Typical SINAD (signal + noise + distortion/noise + distortion)

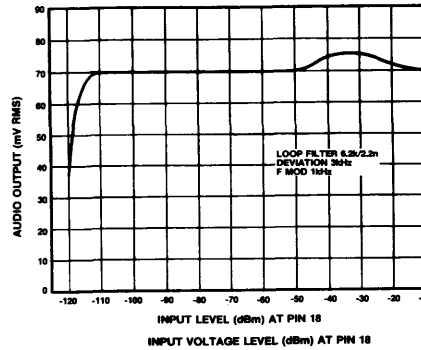

Fig.6 Typical recovered audio v. input level (3kHz deviation)

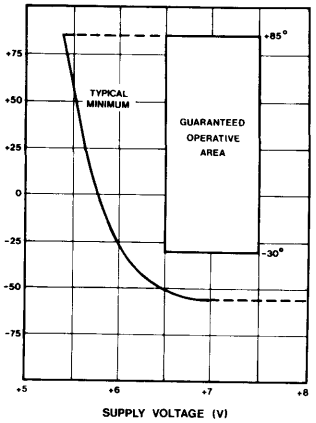

Fig.7 Supply voltage v. temperature

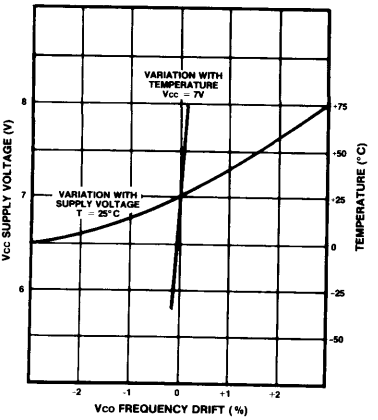

Fig.8 Typical VCO characteristics

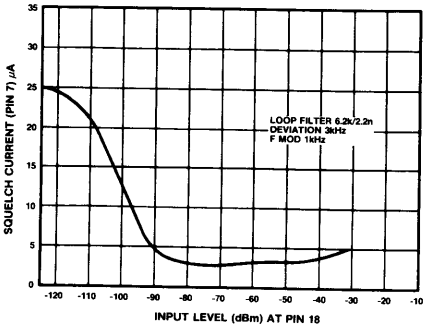

Fig.9 Typical squelch current v. input level

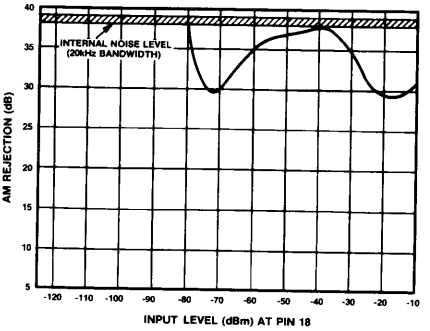

Fig.10 Typical AM rejection

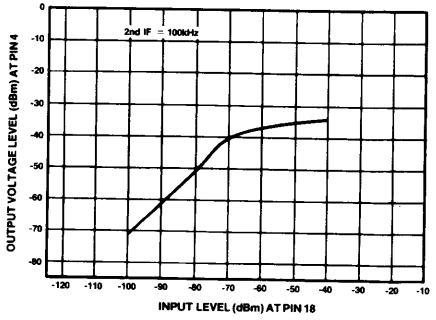

Fig.11 Typical conversion gain (to pin 4)

(the ratio between the audio output produced by:
(a) a 3kHz deviation 1kHz modulation FM signal and
(b) a 30% modulated 1kHz modulation AM signal at the same input voltage level.)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	9V
Storage temperature	-55°C to +125°C (DP package)
	-55°C to +150°C (DG/GC)
Operating temperature (see Electrical Characteristics)	-55°C to +125°C
Input voltage	1V RMS at pin 18

PLESSEY
Semiconductors

SL6691C

MONOLITHIC CIRCUIT FOR PAGING RECEIVERS

The SL6691C is an IF system for paging receivers, consisting of a limiting IF amplifier, quadrature demodulator, voltage regulator and audio tone amplifier with Schmitt trigger.

The voltage regulator requires an external PNP transistor as the series pass transistor. The frequency response of the tone audio amplifier is externally defined.

The SL6691C operates over the temperature range -30° C to +85° C.

FEATURES

- Very Low Standby Current
- Fast Turn-on
- Wide Dynamic Range
- Minimum External Components

APPLICATIONS

- Pagers
- Portable FM Broadcast Receivers

ABSOLUTE MAXIMUM RATINGS

Storage temperature -65°C to +150°C
Supply voltage 6V

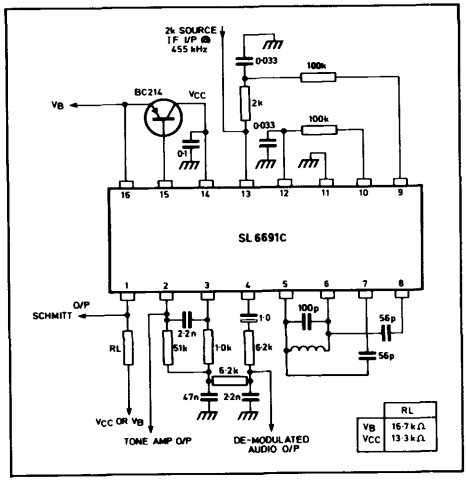

Fig.2 SL6691C test circuit

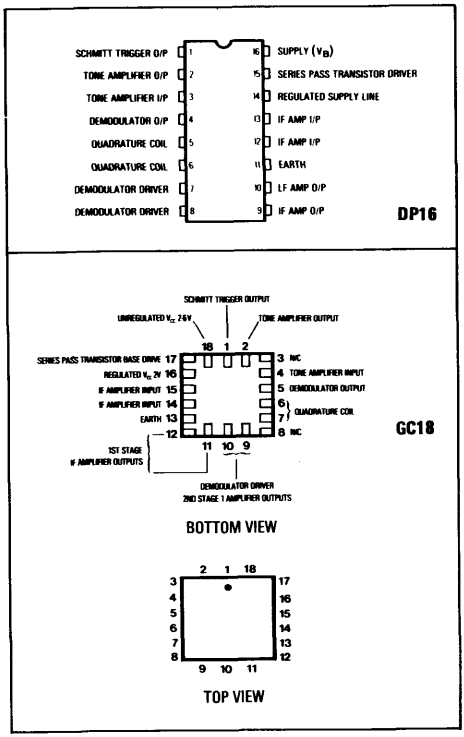

Fig.1 Pin connections (top view)

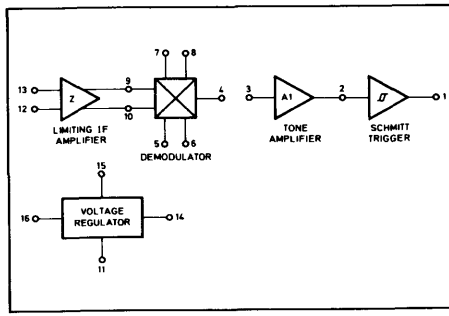

Fig.3 SL6691C block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Temperature	-30°C to +85°C
Supply voltage (V_C)	2.5V
IF frequency	455kHz (nominal)
Modulation frequency	500Hz
Deviation	±4.5kHz

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Quiescent current		1.0	1.4	mA	V_B = 3V Pins 2 and 3 S/C Pins 1 and 4 O/C
Switch on time		12	18	ms	Note 1
Voltage regulator					
Regulated voltage	1.9		2.1	V	V_B > 2.2V
Supply line rejection		40		dB	V_B > 2.2V 200mV p-p square wave @ 500 Hz injected
Current sink capability pin 15	100			µA	
IF amplifier					
Input impedance		20//2		kΩ//pF	
Output impedance		2		kΩ	
Dynamic range		100		dB	
Output voltage swing		600		mV p-p	
Amplifier gain		90		dB	
Sensitivity	20	16		µV rms	Audio 20dB S+N/N ratio
AM rejection		40		dB	100µV rms I/P @ 30% AM modulation
Amplifier 3dB bandwidth		1.5		MHz	
Demodulator					
Audio output	8	15		mV rms	Quadrature element L-C tuned circuit : Q = 30
Distortion, THD		1.5	3	%	
Output impedance		1	3	kΩ	
Signal-to-noise ratio		40		dB	100µV rms I/P 3kHz audio bandwidth
Tone amplifier					
Open loop gain		54		dB	
Peak output current		20		µA	
Schmitt trigger					
Mark space ratio		45/55	38/62		20µV rms I/P
Output current			150	µA	

NOTES

1. The 'Switch On' time is the time to the zero crossing point of the centre of the first occurrence of a 30/70 or 70/30 mark space wave on the output of the Schmitt trigger after the supply voltage has been switched on. Conditions: V_B = 2V, Tone filter connected (See Fig.2), IF input = 100µV rms, Modulation 500 Hz @ 2kHz deviation.

CIRCUIT DESCRIPTION

IF Amplifier and Detector

The IF amplifier consists of five identical differential amplifier/emitter follower stages with outputs at the fourth (pins 9 and 10) and fifth (pins 7 and 8) stages. The outputs from the fourth stage are used when the lowest turn-on time is required. Coupling to the quadrature network of the detector is via external capacitors; otherwise the design is conventional. The audio output is taken from pin 4 and filtered externally.

Tone (Audio) Amplifier

The tone amplifier is a simple inverting audio amplifier with voltage gain determined by the ratio of feedback resistor to input resistor. The frequency response can readily be controlled by suitable selection of feedback components.

Schmitt Trigger

The Schmitt trigger has an open collector output stage which saturates when the input at pin 2 is high. A 20µV rms input is sufficient.

NOMINAL DC PIN VOLTAGES(DP16)

Function	Pin	Voltage
Supply	16	Battery voltage
Series pass transistor driver	15	Battery voltage –0.7V
Regulated supply line	14	2V
Earth	11	0V
IF amp I/P	13	1V
IF amp I/P	12	1V
IF amp O/P	10	1V
IF amp O/P	9	1V
Demodulator O/P	4	1V
Quadrature coil	6	1V
Quadrature coil	5	1V
Tone amplifier I/P	3	1.4V
Schmitt trigger O/P	1	0V or pin 16 or pin14
Tone amplifier O/P	2	1.4V
Demodulator driver	7	1V
Demodulator driver	8	1V

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SL6700A

IF AMPLIFIER AND AM DETECTOR

The SL6700A is a single or double conversion IF amplifier and detector for AM radio applications. Its low power consumption makes it ideal for hand held applications. Normally the SL6700A will be fed with a first IF signal of 10.7MHz or 21.4MHz; there is a mixer for conversion to the first or second IF, a detector, an AGC generator with optional delayed output and a noise blanker monostable. This device is characterised for operation from -55°C to +125°C.

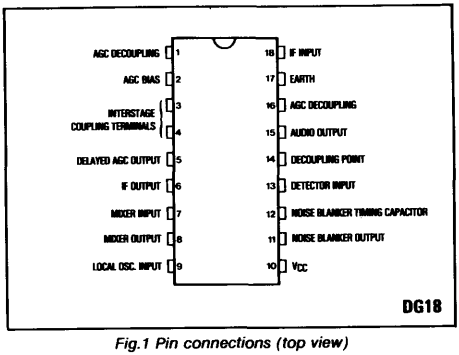

Fig.1 Pin connections (top view)

FEATURES

- High Sensitivity: 10µV Minimum
- Low Power: 8mA Typical at 6V
- Linear Detector
- Full MIL Temperature Range

APPLICATIONS

- Low Power AM/SSB Receivers

QUICK REFERENCE DATA

- Supply Voltage: 4.5V
- Input Dynamic Range: 100dB Typical

ABSOLUTE MAXIMUM RATINGS

Supply voltage	7.5V
Storage temperature	-55°C to +150°C
Operating temperature	-55°C to +125°C

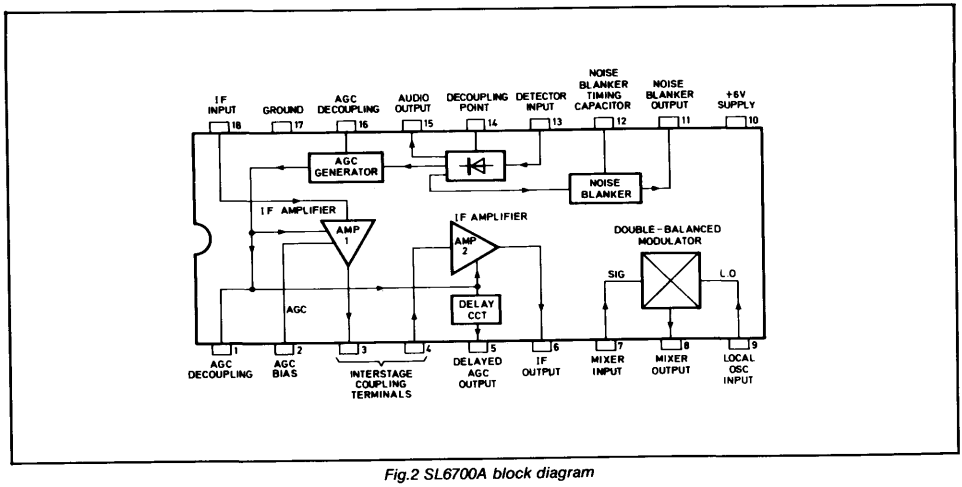

Fig.2 SL6700A block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} -55°C to +125°C Test circuit Fig.6. Modulation frequency 1kHz

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply voltage	4		7	V	Optimum performance at 4.5V
Supply current		3.5	7	mA	
S/N ratio		40		dB	1mV input 80% modulation
TH distortion		3	5	%	1mV input 30% modulation
Sensitivity	10	5		μV	10dB S + N/N ratio, 30%
Audio output level change		6	10	dB	10μV to 50mV input 80%
AGC threshold		5		μV	
AGC range		80		dB	
AF output level	20	40		mV rms	30% modulation 1mV input
Delayed AGC threshold		10		mV rms	80% modulation
Dynamic range		100		dB	Noise floor to overload
IF frequency response	15	25		MHz	3dB gain reduction
IF amplifier gain	40	50	60	dB	10.7MHz (both amplifiers cascaded)
Detector gain	40	46	55	dB	455kHz 80% AM
Detector Z_{in} pin 13	2	4	6.8	kΩ	
IF amplifier Z_{in} pin 18	1.8	3	4.5	kΩ	
Noise blank level	4.0			V	Logic 1
			0.3	V	Logic 0
Noise blank duration	300	400	500	μs	C pin 12 = 30nF,R pin 12-11 = 18k
Mixer conversion gain	1.0R	1.2R	1.5R	kΩ	R is load resistor in kΩ
Mixer Z_{in} (Signal)	2	3	5	kΩ	
Mixer Z_{in} (L.O.)	3	5	8	kΩ	
Mixer L.O. injection	50	100	150	mV rms	fc = 10.245MHz
Detector output voltage change	6	8	8.2	dB	1mV rms input, modulation increased from 30% to 80%

OPERATING NOTES

The noise blank duration can be varied from the suggested value of 30μs using the formula: Duration time = 0.7CR, where R is value of resistor between pins 11 and 12 and C is value of capacitor from pin 12 to ground.

There is no squelch in the SL6700A and the delay in the delayed AGC is too large to make this output suitable. Squelch is best obtained from a comparator on the AGC decoupling point, pin 16.

The IF amplifiers may be operated at 455kHz giving a single conversion system.

The mixer may also be used as a product detector. Further application information is available on request.

The mixer may also be used as a product detector. Further application information is available on request in Application Note AN1001.

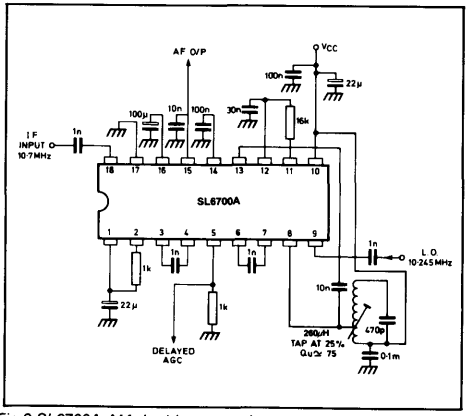

Fig.3 SL6700A AM double conversion receiver with noise blanker

TYPICAL DC PIN VOLTAGES

(Supply 4.5V, Input 1mV)

Pin	Voltage	Pin	Voltage
1	2.25V	10	4.5V
2	2.09V	11	3.7V
3	3.68V	12	0V
4	0.7V	13	0.77V
5	0.6V	14	1.5V
6	3.7V	15	1.0V
7	1.5V	16	0.7V
8	4.3V	17	0V
9	1.5V	18	0.7V

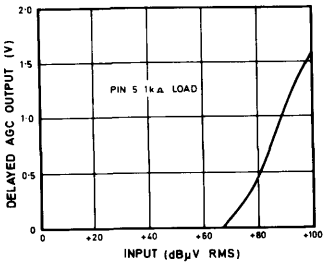

Fig.4 Typical delayed AGC output variation with input signal (f = 10.7MHz, 30% modulation)

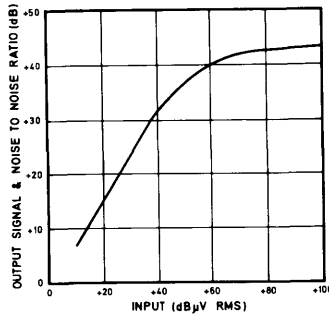

Fig.5 Typical signal to noise ratio (S + N/N) with input signal (f = 10.7MHz, 30% modulation)

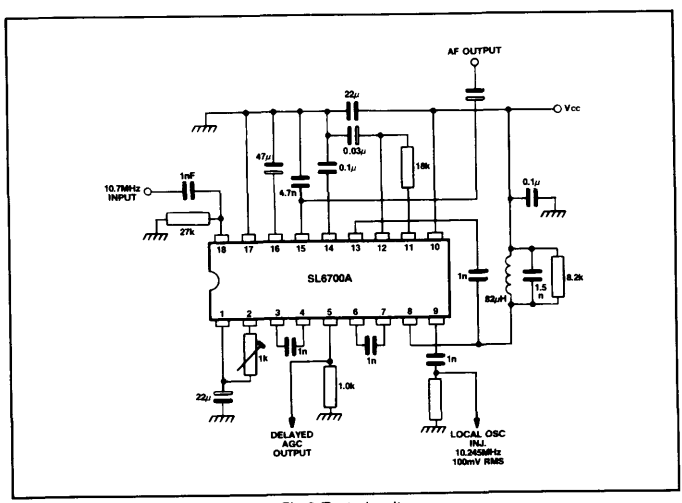

Fig.6 Test circuit

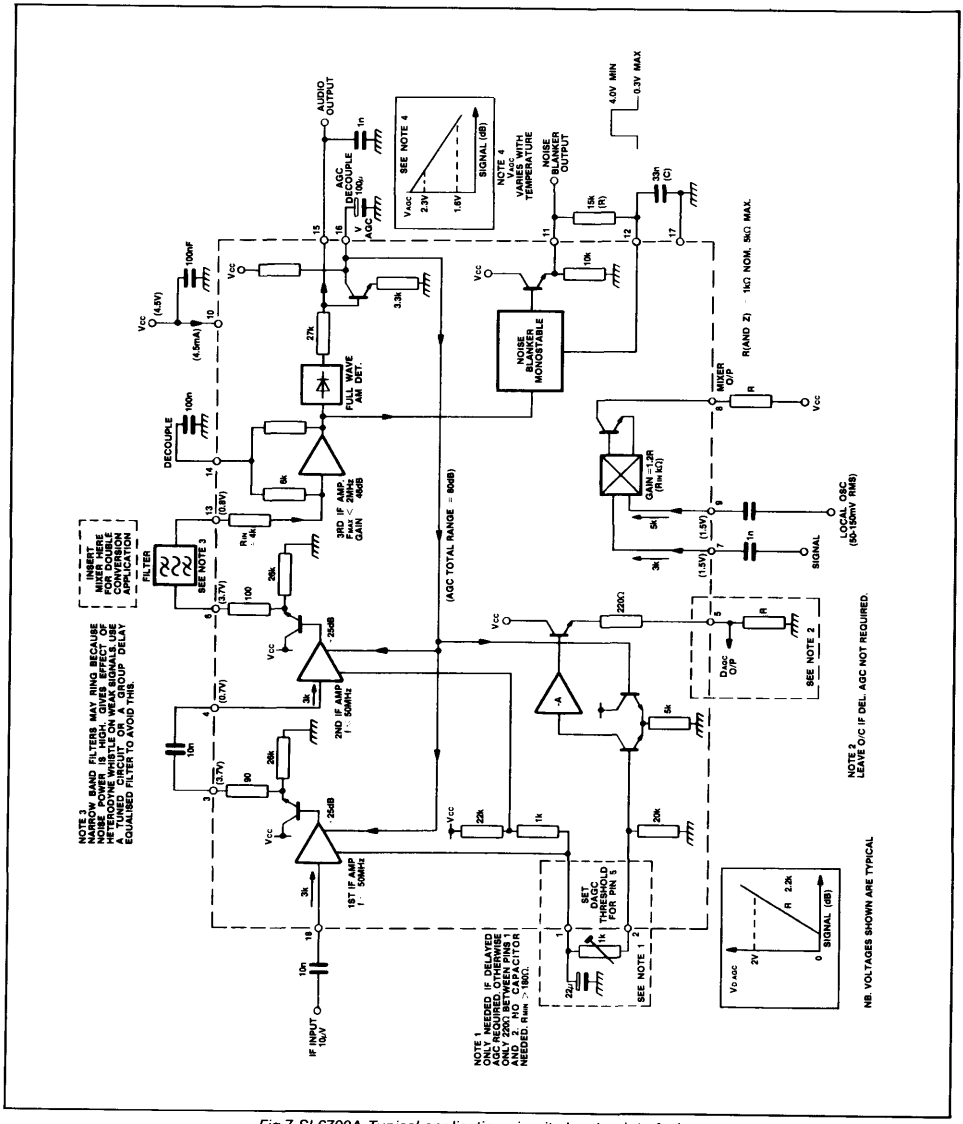

Fig.7 SL6700A Typical application circuit showing interfacing

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ADVANCE INFORMATION

SL6700C

IF AMPLIFIER AND AM DETECTOR

The SL6700C is a single or double conversion IF amplifier and detector for AM radio applications. Its low power consumption makes it ideal for hand held applications. Normally the SL6700C will be fed with a first IF signal of 10.7MHz or 21.4MHz; there is a mixer for conversion to the first or second IF, a detector, an AGC generator with optional delayed output and a noise blanker monostable.

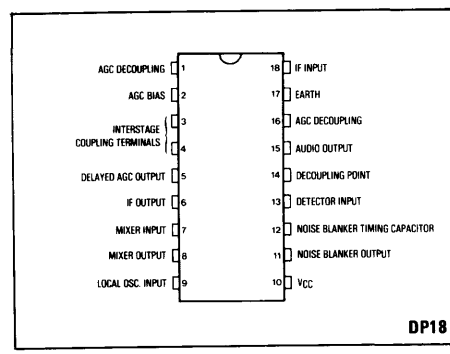

Fig. 1 Pin connections (top view)

FEATURES

- High Sensitivity: 10μV minimum
- Low Power: 8mA Typical at 6V
- Linear Detector

APPLICATIONS

- Low Power AM/SSB Receivers

QUICK REFERENCE DATA

- Supply Voltage: 4.5V
- Input Dynamic Range: 100dB Typical

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 7.5V
Storage temperature: —55°C to +125°C

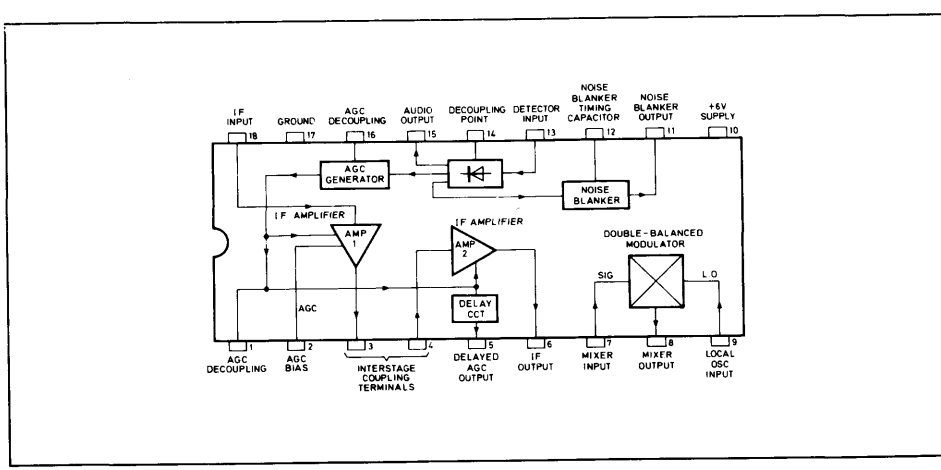

Fig. 2 SL6700C block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage 4.5V
T_{Amb} -30°C to +85°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply voltage	4		7	V	Optimum performance at 4.5V
Supply current		4.5	6	mA	
S/N ratio		40		dB	1mV input 80% mod @ 1kHz
TH distortion		1	5	%	1mV input 80% mod @ 1kHz
Sensitivity	10	5		μV	10dB S + n/N ratio, 30% mod 1kHz
Audio output level change		6	10	dB	10μV to 50mV input 80% mod 1kHz
AGC threshold		5		μV	
AGC range		80		dB	
AF output level		25		mV rms	30 % modulation 1kHz
Delayed AGC threshold		10		mV rms	80 % modulation
Dynamic range		100		dB	Noise floor to overload
IF frequency response	40	50		MHz	3dB gain reduction
IF amplifier gain	40	50	60	dB	10.7MHz (both amplifiers cascaded)
Detector gain	40	46	55	dB	455kHz 80 % AM 1kHz
Detector Z_{in} pin 13	2	4	6.8	kΩ	
IF amplifier Z_{in} pin 18	1.8	3	4.5	kΩ	
Noise blank level	2.7			V	Logic 1
			0.6	V	Logic 0
Noise blank duration		300		μs	C pin 12 = 30nF
Mixer conversion gain	1.0R	1.2R	1.5R	kΩ	R is load resistor in kΩ
Mixer Z_{in} (signal)	2	3	5	kΩ	
Mixer Z_{in} (LO)	3	5	8	kΩ	
Mixer LO injection	20	50	150	mV rms	fc = 10.245MHz
Detector output voltage change	6	8	8.2	dB	1mV rms input, 1kHz modulation increased from 30 % to 80 %

OPERATING NOTES

The noise blank duration can be varied from the suggested value of 300μs using the formula: Duration time = 0.7CR, where R is value of resistor between pins 11 and 12 and C is value of capacitor from pin 12 to ground.

There is no squelch in the SL6700C and the delay in the delayed AGC is too large to make this output suitable. Squelch is best obtained from a comparator on the AGC decoupling point, pin 16.

The IF amplifiers may be operated at 455kHz giving a single conversion system.

The mixer may also be used as a product detector. Further application information is available in Application Note AN1001.

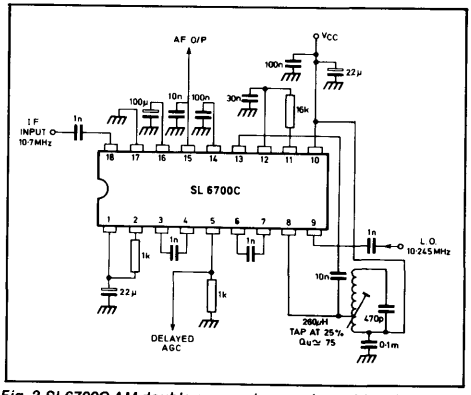

Fig. 3 SL6700C AM double conversion receiver with noise blanker

TYPICAL DC PIN VOLTAGES
(Supply 4.5V, Input 1mV)

Pin	Voltage	Pin	Voltage
1	2.25V	10	4.5V
2	2 09V	11	3.7V
3	3.68V	12	0V
4	0.7V	13	0.77V
5	0.6V	14	1.5V
6	3.7V	15	1.0V
7	1.5V	16	0.7V
8	4.3V	17	0V
9	1.5V	18	0.7V

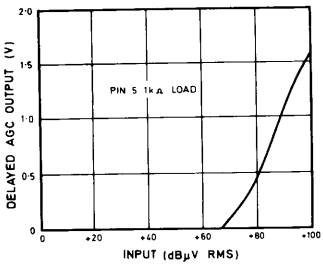

Fig. 4 Typical delayed AGC output variation with input signal (f=10.7MHz, 30% modulation)

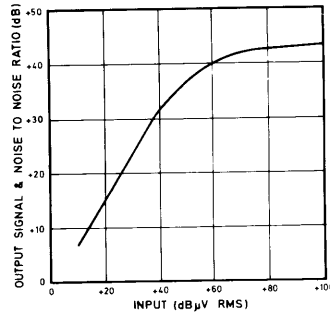

Fig. 5 Typical signal to noise ratio (S+N/N) with input signal (f=10.7MHz, 30% modulation)

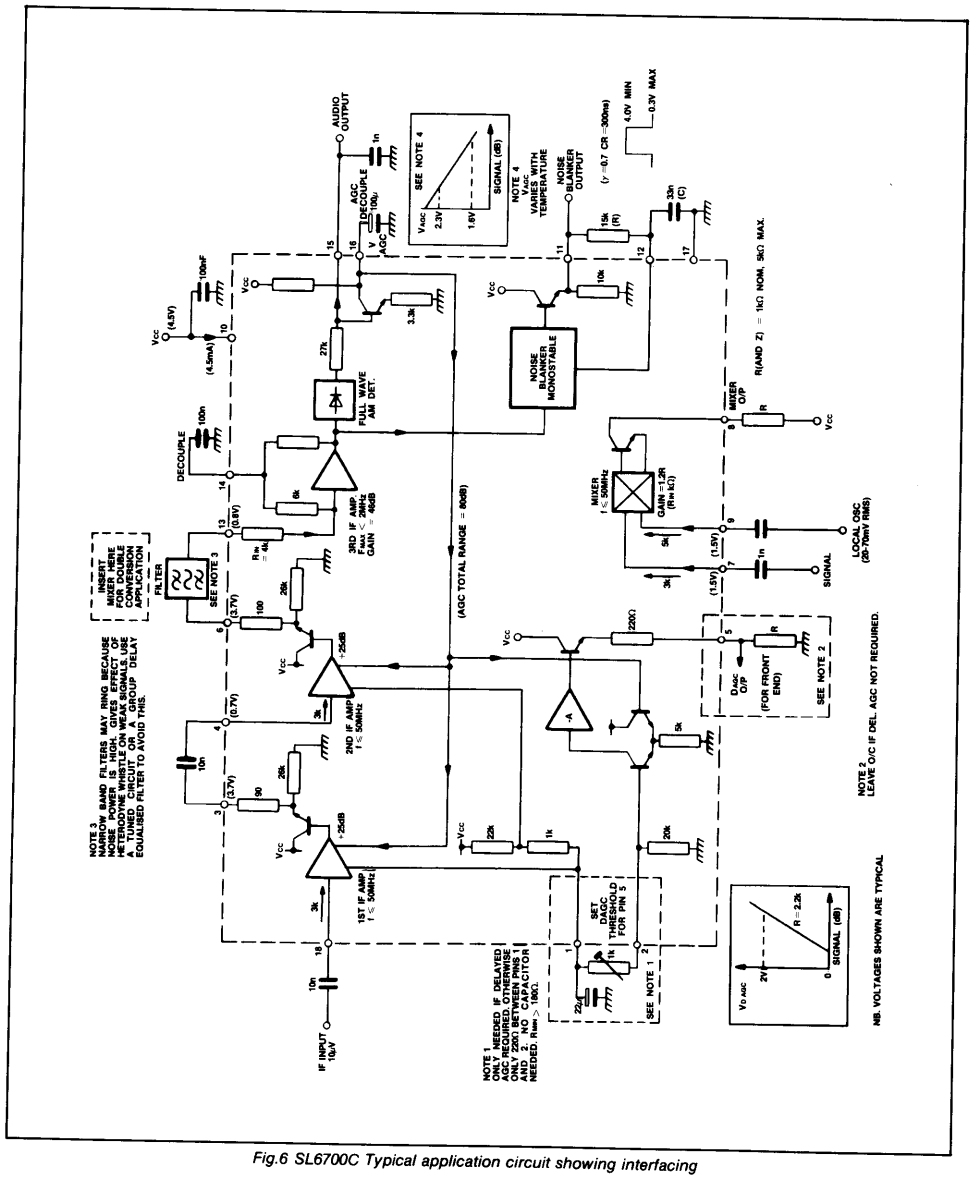

Fig.6 SL6700C Typical application circuit showing interfacing

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TAB1042

QUAD PROGRAMMABLE OPERATIONAL AMPLIFIER

The TAB1042 is an advanced bipolar integrated circuit containing four separate programmable operational amplifiers. The four amplifiers are programmed by current into a common bias pin which determines the main characteristics of each amplifier, supply current, frequency response and slew rate.

For example, with a suitable choice of bias current, the TAB1042 will perform in a manner similar to four amplifiers of the 741 type, but with improved frequency response and input characteristics.

The TAB1042 is especially suitable for use in active filter applications.

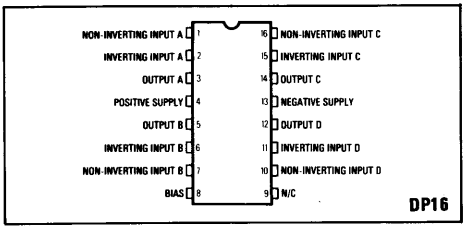

Fig. 1 Pin connections

FEATURES

- Four Independent Op. Amps. in One Package
- Internally Compensated
- Wide Range of Supply Voltages from ±1.5V to ±12V
- No Latch-Up
- Programmable Over 100:1 Current Range
- Gain Bandwidth Product Up to 4MHz
- Built-In Short Circuit Protection
- Low Noise

APPLICATIONS

- Active Filters
- Oscillators
- Low Voltage Amplifiers

QUICK REFERENCE DATA

- Supply Voltages ±1.5V to ±12V
- Supply Current ±40uA to ±2mA
- Operating Frequency Range 1MHz
- Gain 95dB
- Operating Temperature Range -40°C to +85°C

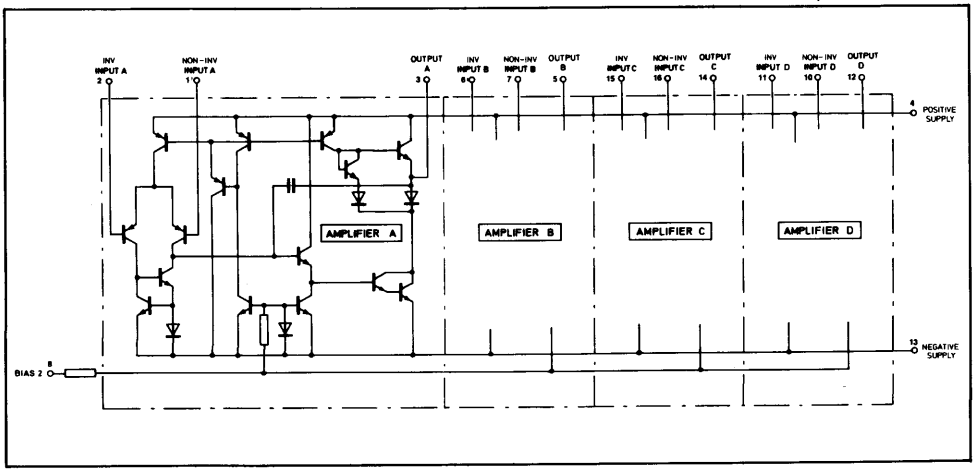

Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} 25°C
Operating mode A:Supply volts ±12V Bias set current 75μA
Operating mode B:Supply volts ±12V Bias set current 1μA
Operating mode C:Supply volts ±1.5V Bias set current 1μA

Characteristics	Operating Mode									Units	Conditions
	A			B			C				
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Input offset voltage		1	5		1	5		1	5	mV	Rs 10kΩ
Input offset current		20	200		5	50		5	50	nA	
Input bias current		250	500		30	100		30	100	nA	
Input resistance	0.1	0.6		0.5	2		0.5	2		MΩ	
Supply current	1000	1600	2200		42		20	40	60	μA	
Large signal volt gain	74	95		66	90		66	90		dB	RL = 4kΩ(A)
											RL = 100kΩ(B)
											RL = 100kΩ(C)
Input voltage range	10	10.5		10	10.5		0.2	0.4		±V	Rs 10kΩ
Common mode rejection ratio	70	110			82			82		dB	
Output voltage swing	9	10.8		9	10.8		0.2	0.3		±V	RL = 4kΩ(A)
											RL = 100kΩ(B)
											RL = 4kΩ(C)
Supply voltage rejection ratio	75	96		75	86		75	86		dB	Rs 10kΩ
Short circuit current	2.5	4		0.1	0.25			0.22		mA	T_{amb} 0°C to 70°C
Gain bandwidth product					50			50		kHz	Gain = 20dB
		3.5								MHz	
Slew rate		1.5			0.02			0.02		V/μs	Gain = 20dB
Input noise voltage		15			45			45		nV/√Hz	f_o = 1kHz
Input noise current		1.6			1.6			1.0		pA/√Hz	f_o = 1kHz

OPERATING NOTES

Bias set current

The amplifiers are programmed by the I_{SET} current into the BIAS pin to determine the frequency response, slew rate and the value of supply current. The relationship is summarised as follows:

Gain bandwidth product	I_{SET} x 50kHz
Power supply current (each supply)	I_{SET} x 25μA
Slew rate	I_{SET} x 0.02 V/μs (I_{SET} in μA)

The open loop voltage gain is largely unaffected by change in bias set current but tends to peak slightly at 10μA.

Since the voltage on the BIAS pin is approximately 0.65V more positive than the negative supply, a resistor may be connected between the bias pin and either 0V or the positive supply to set the current. Thus, if the resistor is connected to 0V, the I_{SET} current is determined by:

$$I_{SET} = \frac{Vs - 0.65}{R}$$

where R is value of the 'set' resistor.

The output goes high if the non-inverting input is taken lower than 1V above the negative power supply.

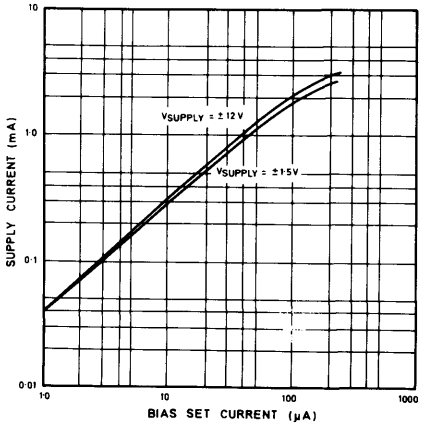

Fig. 3 Supply current (each supply) v. bias set current

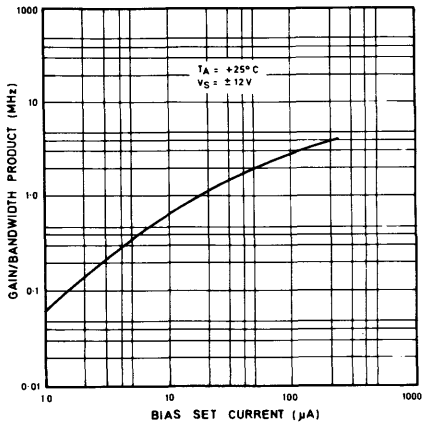

Fig. 4 Gain bandwidth product v. I_{SET}

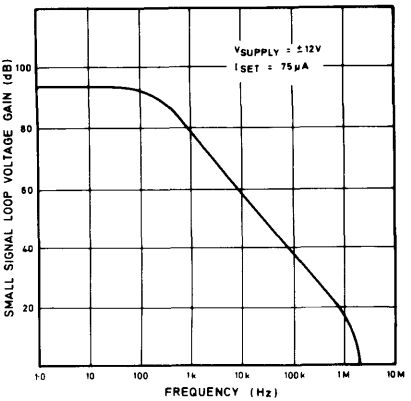

Fig. 5 Typical frequency response

ABSOLUTE MAXIMUM RATINGS

Supply voltages	±15V
Common mode input voltage	Not greater than supplies
Differential input voltage	±25V
Bias set current	10mA each pin
Storage	-55° C to +125° C
Power dissipation	800mW at 25° C
	Derate at 7mW/° C above 25° C
Operating temperature range	-40° C to +85° C

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TAB 1043

QUAD PROGRAMMABLE OPERATIONAL AMPLIFIER

The TAB1043 is an advanced bipolar integrated circuit containing four separate operational amplifiers. The amplifiers are programmed by current into the appropriate bias pin. Pin 8 (Bias 2) programmes amplifiers B, C and D and pin 16 (Bias 1) programmes amplifier A.

For example, with a suitable choice of bias current, the TAB1043 will perform in a manner similar to four amplifiers of the 741 type, but with improved frequency response and input characteristics.

The TAB1043 is especially suitable for use in active filter applications.

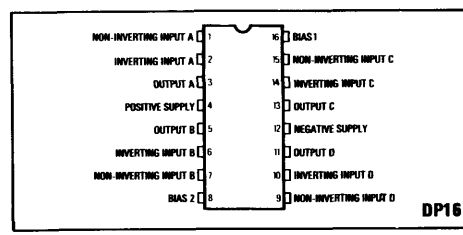


Fig. 1 Pin connections

FEATURES

- Four Independent Op. Amps. in One Package
- Internally Compensated
- Wide Range of Supply Voltages from ±1.5V to ±12V
- No Latch-Up
- Programmable Over 100:1 Current Range
- Gain Bandwidth Product Up to 4MHz
- Built-In Short Circuit Protection
- Low Noise

APPLICATIONS

- Active Filters
- Oscillators
- Low Voltage Amplifiers

QUICK REFERENCE DATA

- Supply Voltages ±1.5V to ±12V
- Supply Current ±40uA to ±2mA
- Operating Frequency Range 1MHz
- Gain 95dB
- Operating Temperature Range -40°C to +85°C

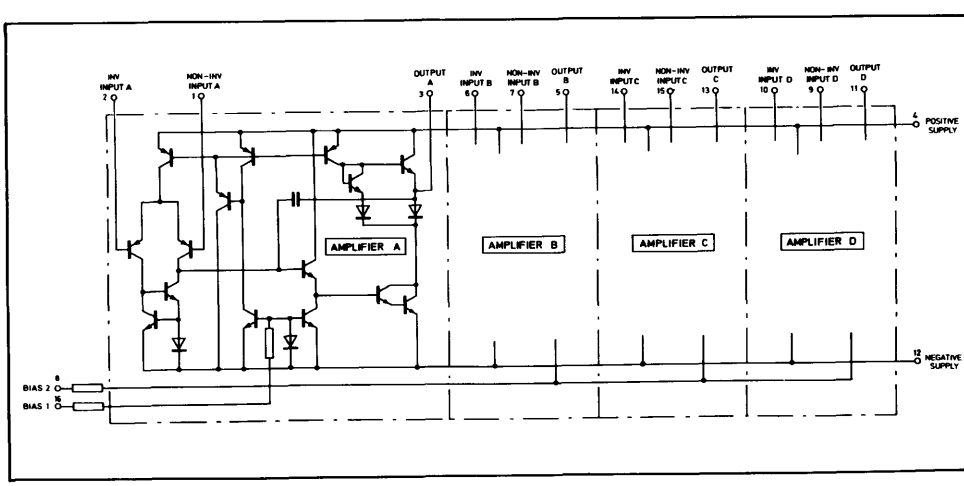


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} 25°C
Operating mode A:Supply volts ±12V Bias set current 75μA
Operating mode B:Supply volts ±12V Bias set current 1μA
Operating mode C:Supply volts ±1.5V Bias set current 1μA
} sum of currents into pins 8 and 16

Characteristics	Operating Mode									Units	Conditions
	A			B			C				
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Input offset voltage		1	5		1	5		1	5	mV	Rs 10kΩ
Input offset current		20	200		5	50		5	50	nA	
Input bias current		250	500		30	100		30	100	nA	
Input resistance	0.1	0.6		0.5	2		0.5	2		MΩ	
Supply current	1000	1700	2500		220		100	200	400	μA	
Large signal volt gain	74	95		66	90		66	90		dB	RL = 4kΩ(A)
											RL = 100kΩ(B)
											RL = 100kΩ(C)
Input voltage range	10	10.5		10	10.5		1.5	1.7		±V	Rs 10kΩ
Common mode rejection ratio	70	110			82			82		dB	
Output voltage swing	9	10.5		9	10.5		0.7	0.8		±V	RL = 4kΩ(A)
											RL = 100kΩ(B)
											RL = 100kΩ(C)
Supply voltage rejection ratio	75	96		75	86		75	86		dB	Rs 10kΩ
Short circuit current	12	20		1.1	2.5		1.0	2.2		mA	T_{amb} 0°C to 70°C
Gain bandwidth product					50			50		kHz	Gain = 20dB
		3.5								MHz	
Slew rate		1.5			0.02			0.02		V/μs	Gain = 20dB
Input noise voltage		15			45			45		nV/√Hz	f_o = 1kHz
Input noise current		1.6			1.6			1.0		pA/√Hz	f_o = 1kHz

OPERATING NOTES

Bias set current

The amplifiers are programmed by the I_{SET} current into the BIAS pins to determine the frequency response, slew rate and the value of supply current. The relationship is summarised as follows, where I_{SET} is the total set current into pins 8 and 16:

Gain bandwidth product	I_{SET} x 50kHz
Power supply current (each supply)	I_{SET} x 25μA
Slew rate	I_{SET} x 0.02 V/μs (I_{SET} in μA)

The open loop voltage gain is largely unaffected by change in bias set current but tends to peak slightly at 10μA.

Since the voltage on either BIAS pin is approximately 0.65V more positive than the negative supply, a resistor may be connected between the bias pin and either 0V or the positive supply to set the current. Thus, if the resistor is connected to 0V, the I_{SET} current is determined by:

$$I_{SET} = \frac{Vs - 0.65}{R}$$

where R is value of the 'set' resistor.

The output goes high if the non-inverting input is taken lower than 1V above the negative power supply.

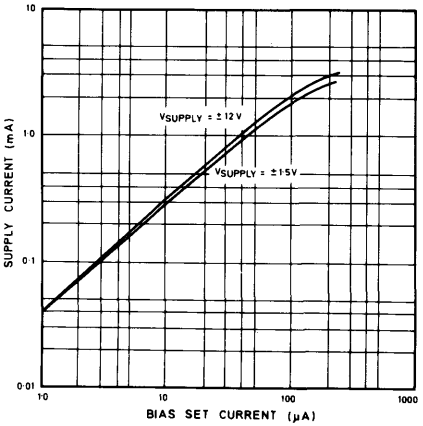


Fig. 3 Supply current (each supply) v. bias set current

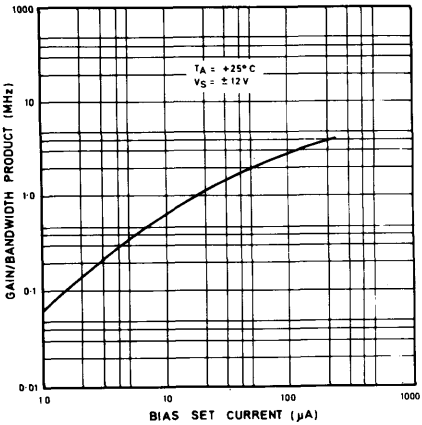


Fig. 4 Gain bandwidth product v. I_{SET}

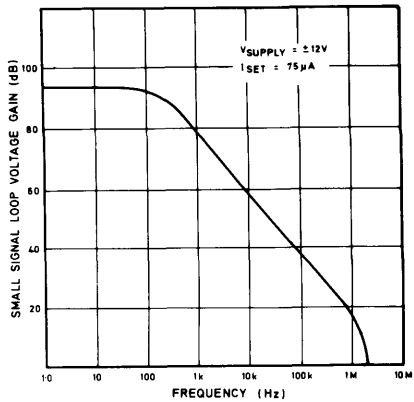
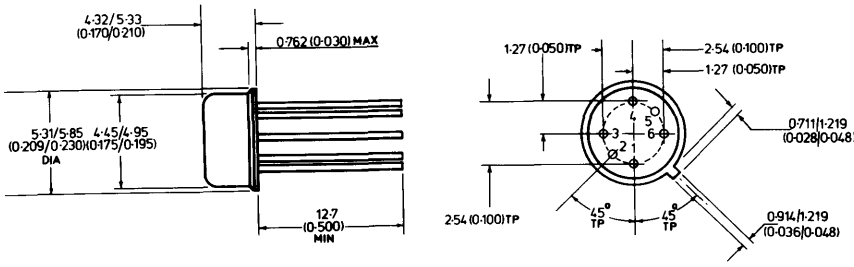


Fig. 5 Typical frequency response

ABSOLUTE MAXIMUM RATINGS

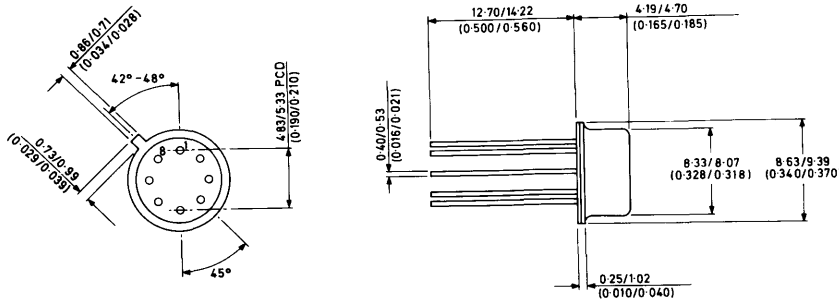
Supply voltages	±15V
Common mode input voltage	Not greater than supplies
Differential input voltage	±25V
Bias set current	10mA
Storage	-55° C to +125° C
Power dissipation	800mW at 25° C
	Derate at 7mW/° C above 25° C
Operating temperature range	-40° C to +85° C

Package Outlines



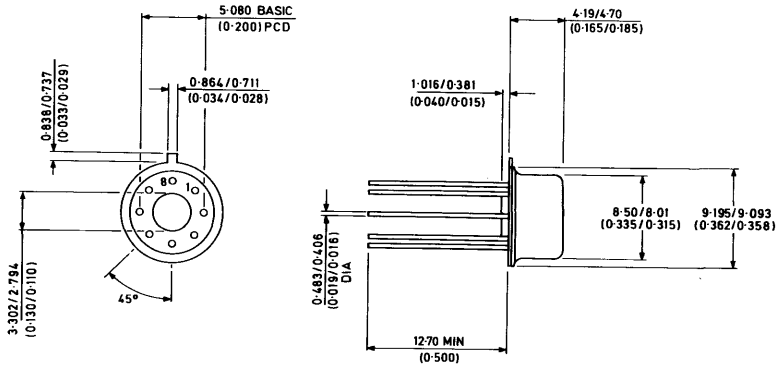
6 LEAD TO-71

CM6



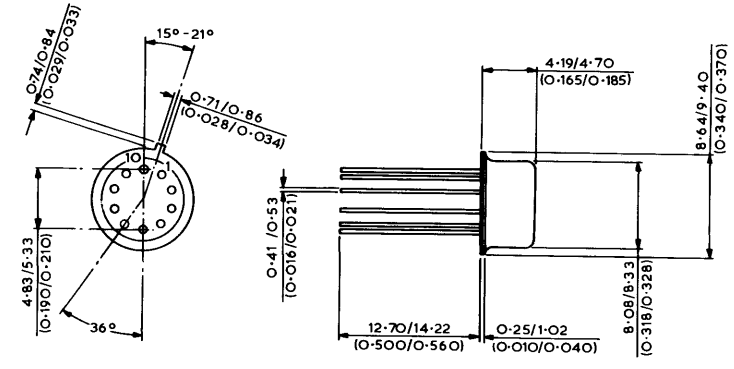
8 LEAD TO-5

CM8



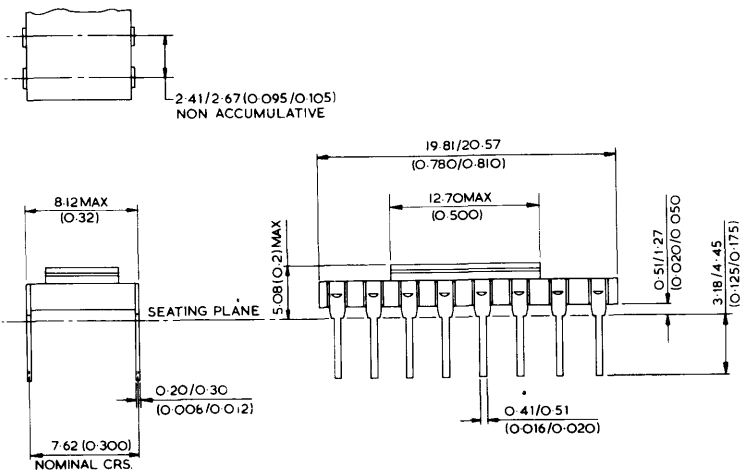
8 LEAD TO-5 WITH STANDOFF

CM8/S



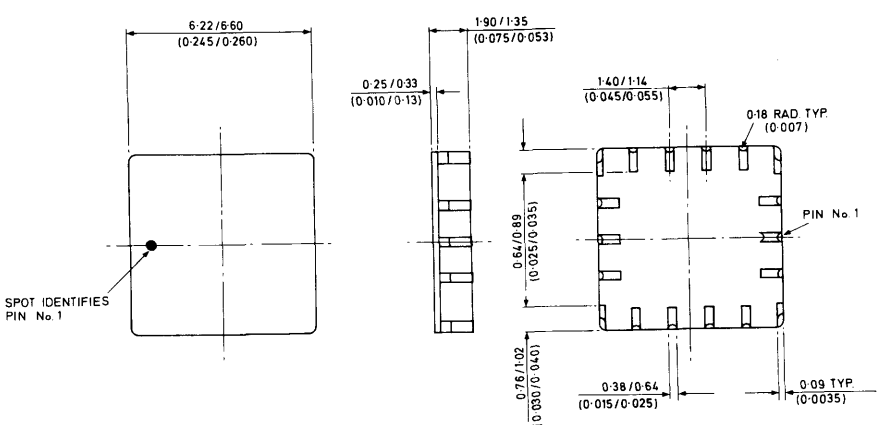
10 LEAD TO-5

CM10



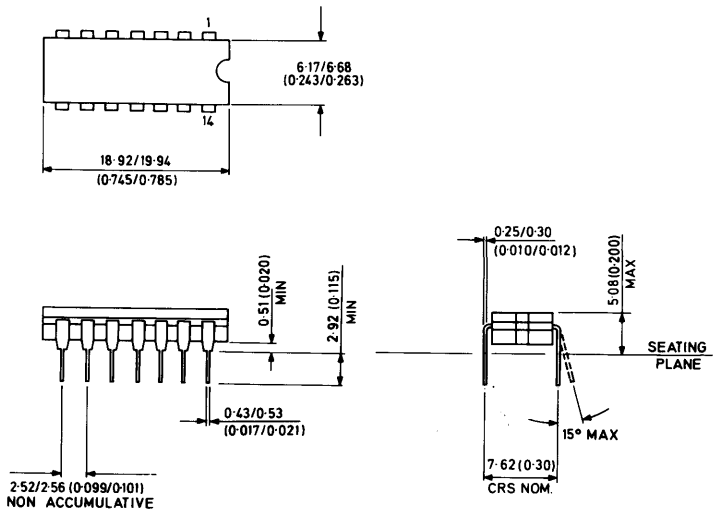
16 LEAD DILMON

DC16



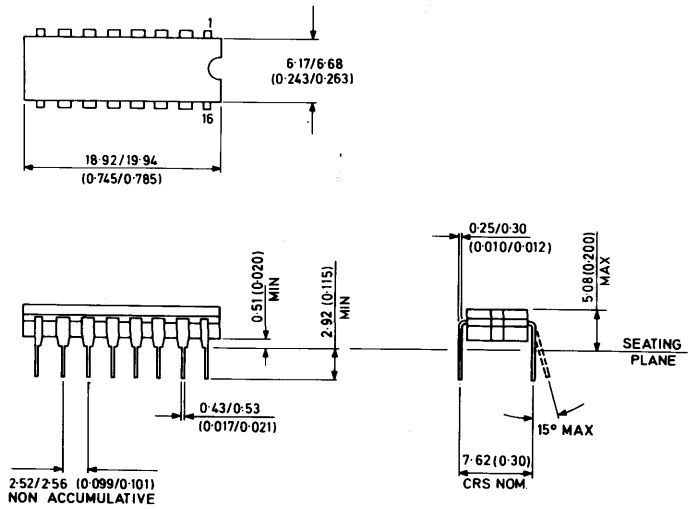
CERAMIC CHIP CARRIER

GC18



14 LEAD CERAMIC DIL

DG14



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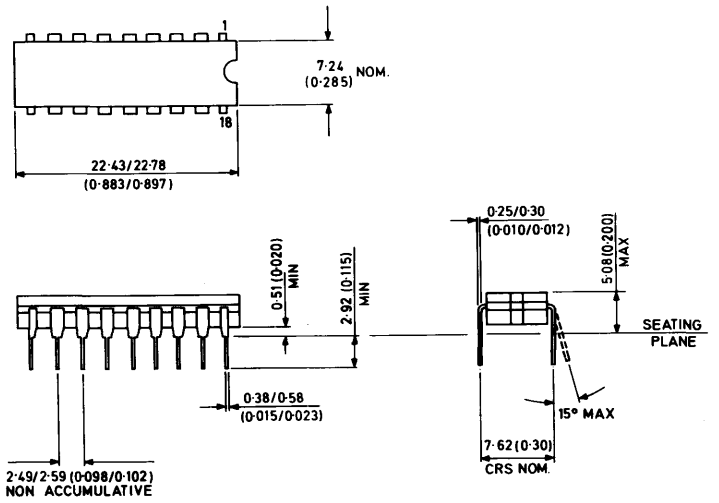

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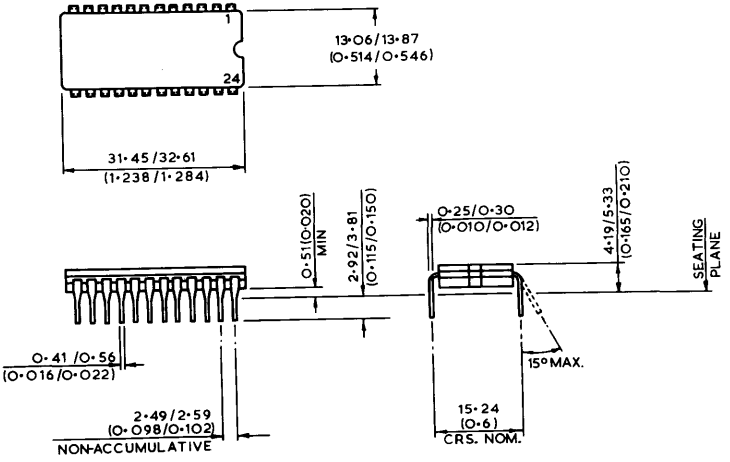

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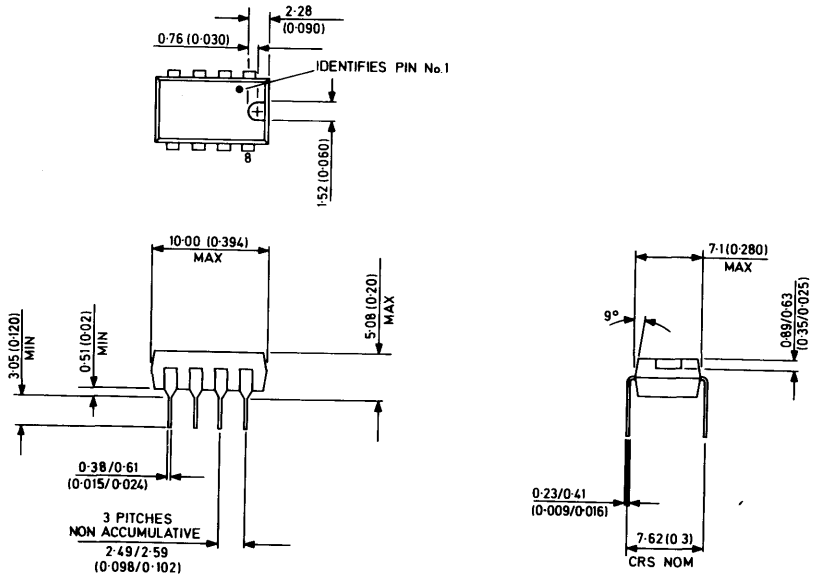
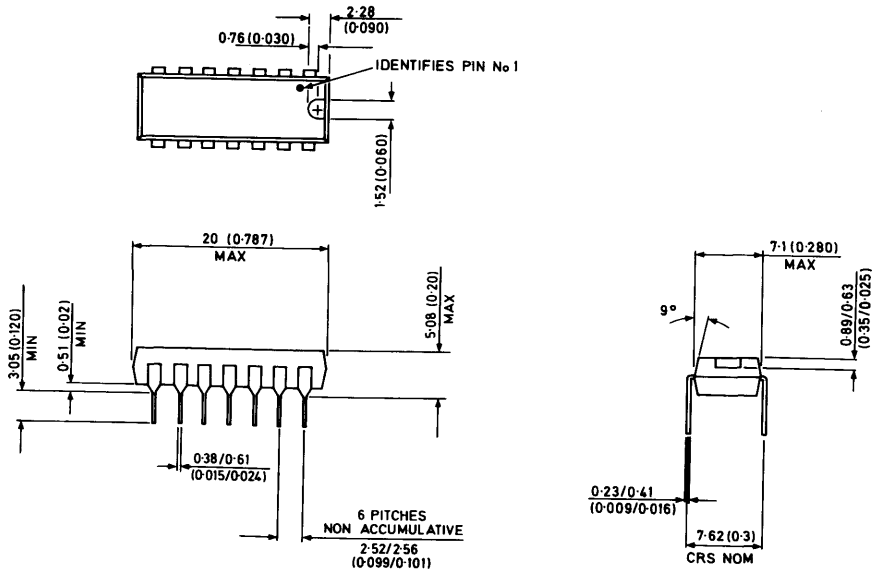
DG24



8 LEAD PLASTIC DIL

DP8



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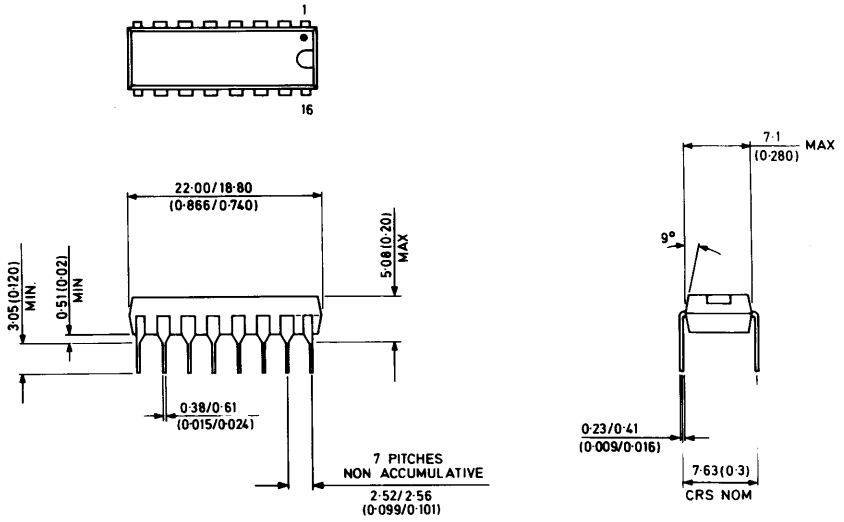
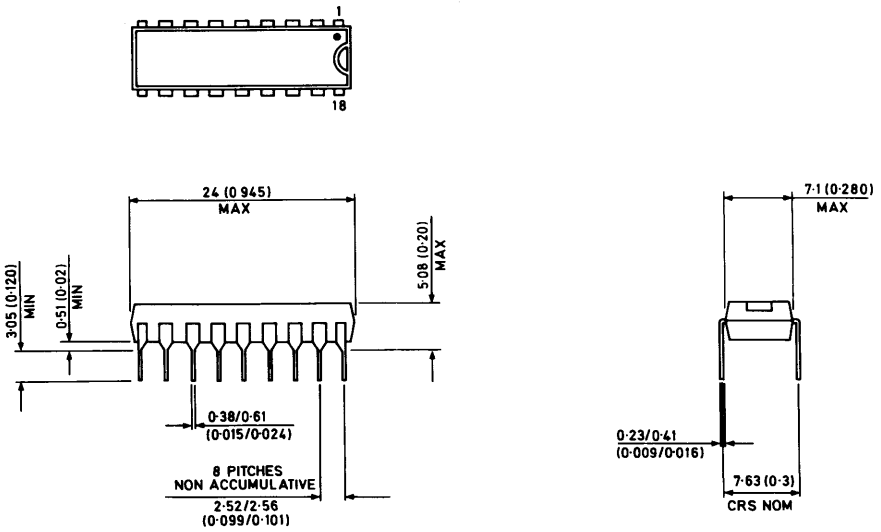


16 LEAD PLASTIC DIL **DP16**



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